SOLID-STATE TERAHERTZ AND MILLIMETER-WAVE ELECTRONICS: REACHING THE FUNDAMENTAL LIMITS

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SOLID-STATE TERAHERTZ AND MILLIMETER-WAVE ELECTRONICS:

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There is a growing interest in terahertz and mm-wave systems for compact, low cost and energy efficient imaging and spectroscopy. Detection of concealed weapons, cancer diagnosis, food quality control, and breath analyses for disease diagnosis are among many examples that will rapidly flourish if compact and on-chip terahertz systems are realized. There are few implementations of terahertz building blocks using compound semiconductors at lower terahertz range. Unfortunately, these processes have low yield, are cost inefficient, and are not suitable for integration of digital blocks on the same chip. On the other hand, while CMOS can overcome these challenges, the best reported f_{max} of CMOS transistors fall well below terahertz frequencies.

To overcome these drawbacks, we have introduced systematic methodologies for designing circuits and components operating close to and beyond the conventional limits of the devices. These circuit blocks can effectively generate, combine, and process signals from multiple devices to achieve performances orders of magnitude better than the state of the art. The proposed techniques are general and can be used in any technology, including CMOS and other processes.

As an example, in Chapter 1 we show a traveling-wave frequency multiplier for high power and wide-band terahertz and mm-wave signal generation. It takes advantage of standing-wave formation and loss cancelation in a distributed structure to generate high amplitude signals resulting in high harmonic power. Wide bandwidth operation and odd harmonic cancelation around the center frequency are the inherent properties of this

frequency multiplier. Using this methodology, we implemented a frequency doubler that operates from 220 GHz to 275 GHz in a standard 65 nm CMOS process. Output power of -6.6 dBm (0.22 mW) and conversion loss of 11.4 dB are measured at 244 GHz. This signal source has twice the operating frequency and tuning range of the best reported CMOS multiplier and 10 times higher output power than the best reported CMOS realization.

In Chapter 2 a systematic approach to designing high frequency and high power oscillators using activity condition is introduced. This method finds the best topology to achieve frequencies close to the f_{max} of the transistors. It also determines the maximum frequency of oscillation for a fixed circuit topology, considering the quality factor of the passive components. Using this technique, in a 0.13 μm CMOS process, we design and implement 121 GHz and 104 GHz fundamental oscillators with the output power of -3.5 dBm and -2.7 dBm, respectively. Next, we introduce a novel triple-push structure to realize 256 GHz and 482 GHz oscillators. The 256 GHz oscillator was implemented in a 0.13 μm CMOS process and the output power of -17 dBm was measured. The 482 GHz oscillator generates -7.9 dBm (160 μW) in a 65 nm CMOS process which is 8,000 times more than any other CMOS sources at this frequency range.

A systematic method to design high gain amplifiers at frequencies close to the f_{max} of the transistors is introduced in Chapter 3. This approach finds the optimum termination conditions to reach the maximum achievable gain of the device. Using this technique in a standard 130 nm CMOS process, we design and implement a 107 GHz amplifier with a gain of 12.5 dB, PAE of 4.4%, and saturated output power of >2.3 dBm, consuming 31 mW from a 0.95 V supply. The center frequency of this amplifier is higher than any other reported amplifier in 130 nm and 90 nm CMOS process. Other specifications such as gain and PAE is comparable to amplifiers in 65 nm CMOS process while consuming 1/3 of the DC power.

Moreover, to go beyond the conventional limitations of passive circuits, we develop a method to perform signal processing using 2-D electrical lattices in Chapter 4. The rich 2-D propagation properties of the medium are used to introduce a novel, high quality factor filter called an *electrical prism* which is compatible with today's conventional integrated circuit processes. The proposed filter shows a quality factor much larger than the quality factor of the individual components at high mm-wave and terahertz frequencies. This structure also provides a negative effective index in a low pass *LC* lattice. Based on this idea, we show filters with quality factors of 130 at 230GHz and 420 at 460GHz consisting of elements with the quality factor of 10 and 20 respectively. The negative effective index and the filter behavior of the lattice is verified by measuring a prototype on a CMOS process at 32GHz-40GHz.

BIOGRAPHICAL SKETCH

Omeed Momeni received the B.Sc. degree in Electrical Engineering from Isfahan University of Technology, Isfahan, Iran, and the M.S. degree in Electrical Engineering from University of Southern California, Los Angeles, in 2002 and 2006, respectively. He is currently working toward his Ph.D. degree at Cornell. His research interests include terahertz and mm-wave integrated circuits and systems.

From May 2004 to December 2006, he was with the National Aeronautics and Space Administration (NASA), Jet Propulsion Laboratory (JPL), to design L-band transceivers for synthetic aperture radars (SAR) and high power amplifiers for Mass Spectrometer applications.

Omeed is the recipient of best PhD thesis award from the school of Electrical and Computer Engineering, Cornell University, best student paper award at the IEEE Workshop on Microwave Passive Circuits and Filters in 2010, the Cornell University Jacobs fellowship in 2007 and the NASA-JPL fellowship award in 2003.

To my Mother and my Wife

for their endless love, patience and support

and to my Son

who has brightened up my life

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I would like to thank my soulmate and my dear wife, Maryam. We have been through a lot during our journey together. She has been my love, my backbone, my inspiration and my best friend. Thank you for being there for me and tolerating all my flaws. I also want to thank my little son, Ilya, who has changed my life and has opened a whole new door for me to enjoy life.

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

A BROADBAND mm-WAVE AND TERAHERTZ TRAVELING-WAVE FREQUENCY MULTIPLIER ON CMOS

1.1 Introduction

Terahertz and high mm-wave frequencies are increasingly used in imaging, spectroscopy, communication and radar systems [1–3]. Detection of concealed weapons, cancer diagnosis, semiconductor wafer/device inspection, vehicular radars, and high data rate communication, along with bio/molecular spectroscopy for explosive and illegal drug detection, food quality control, and breath analysis for disease diagnosis are among many applications in these frequency ranges [4–8].

High power tunable signal sources are one of the most challenging parts of these systems. Voltage controlled oscillators (VCO) are widely used as tunable signal sources at lower frequencies. However, at terahertz and high mm-wave frequencies, solid-state VCO's suffer from high phase noise, low output power and low tuning range. This is mainly due to the low quality factor of varactors as well as the poor transistor gain at these frequencies [9]. To alleviate these drawbacks, frequency multipliers using diodes or transistors are commonly employed. Schottky diode is the most popular device in diode-based frequency multipliers [10–18]. Due to its structure it is difficult to integrate Schottky diode with other blocks such as amplifiers and oscillators [19]. Moreover, because of the passive nature of diode-based multipliers, the required input power to push the diodes into the nonlinear region is high and therefore the conversion gain is low for low input power levels. Isolation between input and output is another challenge that needs to be addressed in any diode-based multiplier.

On the other hand, transistor-based multipliers can take advantage of the transconductance of the transistor to boost the voltage swing at input and/or output nodes and therefore increase the conversion gain even at low input power levels. Furthermore, using 2-port devices, high input-output isolation can be achieved in these frequency multipliers. Transistor-based multipliers also have the advantage of being easily integrated with other building blocks of the system. This is specially valuable in CMOS as it offers low-cost and reliable fabrication of various analog and digital blocks. CMOS frequency multipliers have been proposed for frequencies below 150 GHz [9, 14–17, 20]. At higher frequencies, multipliers are implemented using III-V-based transistors or silicon-based HBTs [19, 21–24]. Recently, CMOS harmonic VCOs have also been introduced for signal generation at these frequencies [25–27]. However, as discussed, the output power and tuning range is too low to be useful in real applications.

In this paper we introduce a novel wideband frequency multiplier that can effectively generate and combine harmonics in order to achieve high output power at high mm-wave and terahertz frequencies [28]. Using this methodology, a frequency doubler that operates from 220 GHz to 275 GHz was implemented in a 65 nm CMOS process. Output power of 220 μW (-6.6 dBm) and conversion loss of 11.4 dB are achieved at 244 GHz. To the best of our knowledge, this work has twice the operating frequency and tuning range of the fastest CMOS multiplier and has higher output power than any CMOS signal source in this frequency range. The performance of the frequency doubler is comparable with monolithic compound semiconductor frequency multipliers.

The rest of this paper is organized as follows. In Section 1.2 we describe the basic idea and the design procedure of the proposed frequency multiplier. The design, simulation, and measurement procedure and results of the implemented frequency doubler are discussed in Section 1.3. We summarize the paper in Section 1.4.

1.2 Traveling-Wave Frequency Multiplier

1.2.1 The Basic Operation

Figure 1.1 shows the basic idea of the proposed frequency multiplier. The input network is an N-section discrete transmission line which is formed by transistor gate capacitors, C_g, and line inductors, L_g. Two signal sources with the same frequency, $\omega_\circ$, are connected to two ends of this transmission line. The two signals travel in opposite directions and their superposition is applied to the gate of the transistors. Due to nonlinearity, the drain currents contain the harmonics of the input signal. The filtering and matching blocks select the desired harmonic and match the transistors to the load, R_L. Although CMOS transistors are shown in Figure 1.1 as the nonlinear components, any nonlinear device including one-port devices such as varactors or diodes can be used to implement this frequency multiplier. More nonlinear devices such as HBTs would result in stronger harmonic generation and higher output power.

Here we assume the loss of the transmission line is negligible. In Section 1.3.1, we justify this assumption by demonstrating how to cancel most of the loss by creating negative impedance using transistors. With this assumption, the voltage at node n is derived to be

$$V_n(t) = A\cos(\omega_\circ t - kn) + A\cos(\omega_\circ t - k(N-n) - \phi), \tag{1.1}$$

where A is the voltage amplitude of the input sources, N is the number of sections, ϕ is the phase difference between the two signal sources, and k is the signal phase shift per section of the transmission line and is defined as

$$k = \omega_\circ \sqrt{L_g C_g}. \tag{1.2}$$

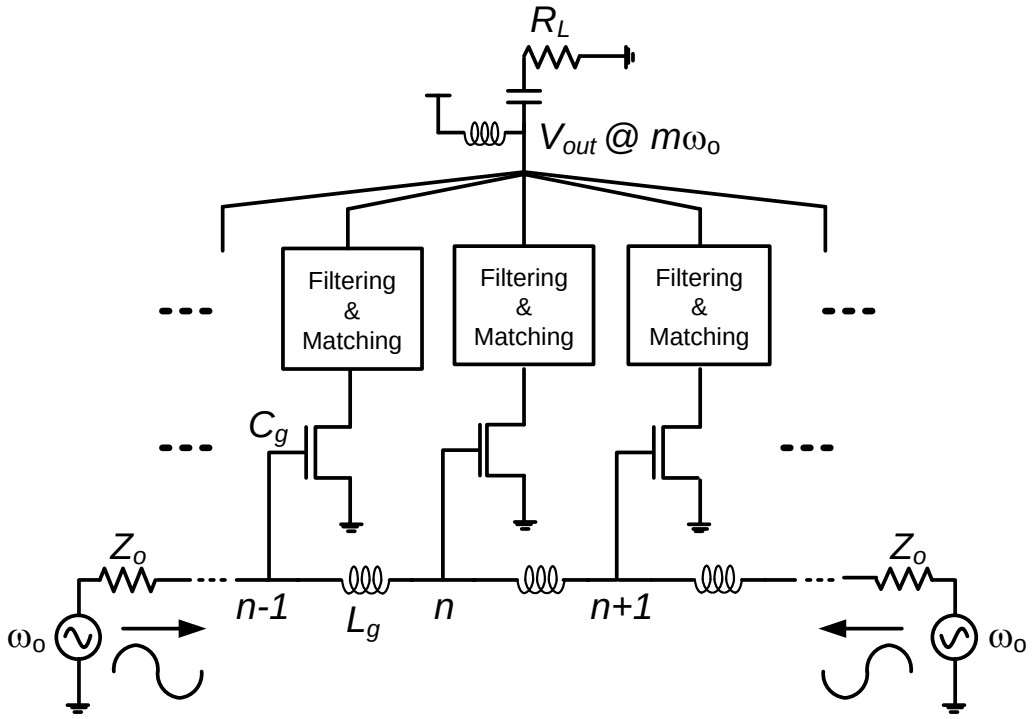


Figure 1.1: Schematic of the traveling-wave frequency multiplier.

We can model the nonlinearity of the transistors by

$$I_{dn}(t) = a_1 V_n(t) + a_2 V_n^2(t) + a_3 V_n^3(t) + a_4 V_n^4(t) \cdots , \tag{1.3}$$

where $I_{dn}(t)$ is the n-th transistor drain current and the a_k's ($k \geq 2$) are the nonlinearity coefficients, which are usually a function of transistor bias point, input signal amplitude, and frequency [29]. By substituting (1.1) in (1.3), the nonlinearity terms of (1.3) can be expanded to be

$$a_1 V_n(t) = 2a_1 A \cos(\frac{1}{2}kN + \frac{1}{2}\phi - kn)\cos(\omega_\circ t - \frac{1}{2}kN - \frac{1}{2}\phi), \tag{1.4a}$$

$$a_2 V_n^2(t) = a_2 A^2[\cos(kN + \phi - 2kn) + 1]\cos(2\omega_\circ t - kN - \phi) + B, \tag{1.4b}$$

$$a_3 V_n^3(t) = a_3 A^3[\frac{3}{2}\cos(\frac{1}{2}kN + \frac{1}{2}\phi - kn) + \frac{1}{2}\cos(\frac{3}{2}kN + \frac{3}{2}\phi - 3kn)]\cos(3\omega_\circ t - \frac{3}{2}kN - \frac{3}{2}\phi) + C, \tag{1.4c}$$

$$a_4 V_n^4(t) = a_4 A^4[\cos(kN+\phi-2kn)+\frac{1}{4}\cos(2kN+2\phi-4kn)+\frac{3}{4}]\cos(4\omega_\circ t-2kN-2\phi)+D, \tag{1.4d}$$

where B is the summation of all the DC components, C is the summation of the DC and fundamental components and D is the summation of the DC and second harmonic components. All the harmonics are in phase from different transistors because their phases are not a function of node number, n. However the signal amplitudes are a function of n and hence may not be the same at different nodes. It is clear from (1.4) that the odd harmonics can have positive and negative amplitudes at different nodes and this will result in destructive power combining. On the other hand, the amplitudes of even harmonics are always positive at different nodes and hence add up constructively in an ideal power combiner. Similarly, by expanding other terms of (1.3), it can be shown that all the other even harmonics (6^{th}, 8^{th}, etc) are always in phase from all the transistors.

Due to frequency independent phase matching, this frequency multiplier has the potential to achieve wide bandwidth and high output power at the same time. Using an ideal power combiner (e.g., putting an antenna at the output of each transistor and add the signals spatially) we can add the output power of all the sections for all the frequencies. Compared to a conventional frequency multiplier (e.g., stand-alone transistor) this frequency multiplier takes advantage of standing wave formation at the gate of the transistors and increases the voltage swing. Doing so we can achieve high power harmonic generation and wide bandwidth operation at the same time. This standing-wave is created by the counter-propagating signals along the input transmission line. As will be discussed in Section 1.2.2, this structure also cancels the odd harmonics around the center frequency which results in a cleaner output spectrum.

Using (1.4), we plot the normalized harmonic amplitudes in a 2-stage multiplier

(i.e., N=2) as a function of k (i.e., frequency) in Figure 1.2. Each harmonic amplitude is normalized to its own nonlinear coefficient, a_k. In this simulation we assume A=1, k=ϕ and the transistors are placed at nodes n=0 and n=1. We will discuss the importance of these conditions in Sections 1.2.2 and 1.2.3. In this simulation we use an ideal power combiner to add the signals from both transistors. For example, using (1.4b) the plotted normalized amplitude of the second harmonic is $\cos(2k + k) + 1 + \cos(2k + k - 2k) + 1$. According to Figure 1.2, if the center frequency is placed at k=π/2, a wide bandwidth for even harmonics and odd harmonic cancelation around the center frequency is achieved. For example, if we assume the center frequency at k=π/2, the input 3-dB bandwidth for the second harmonic is calculated to be $1.27\omega_\circ$ which translates to 127% 3-dB tuning range at input and output.

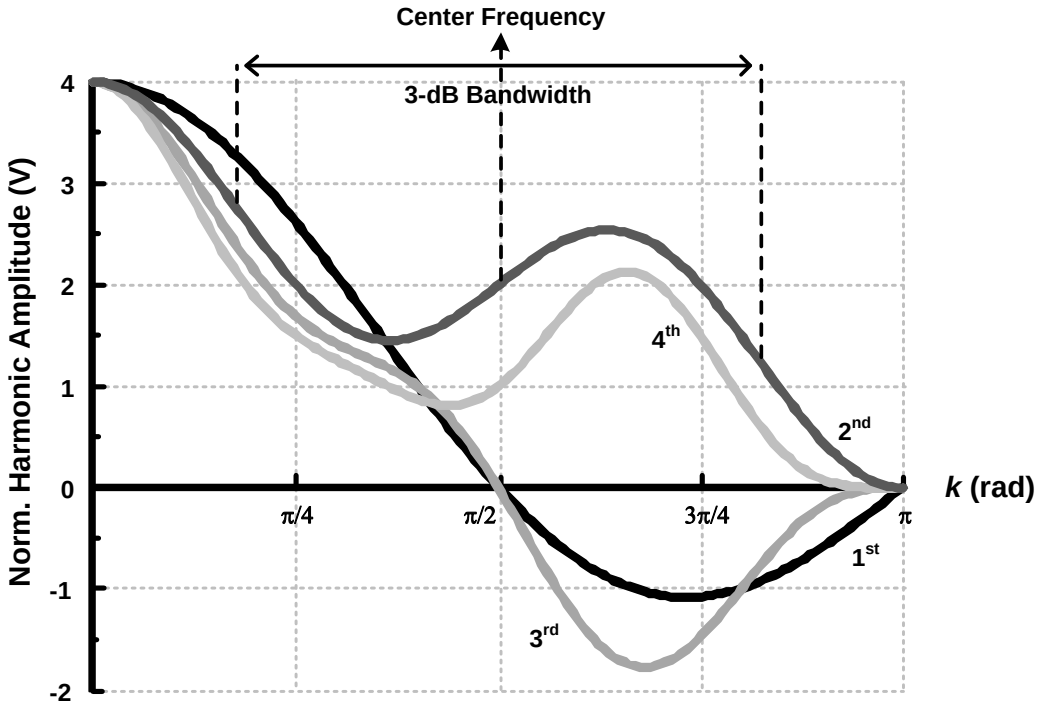


Figure 1.2: Normalized harmonic amplitudes in a 2-stage multiplier as a function of the wavenumber, k.

1.2.2 Odd Harmonic Cancelation

In order to cancel the odd harmonics at the output we need to find the conditions for k and ϕ. One way to do this is to find the conditions in which the amplitudes of all the odd harmonics are zero at all the nodes (e.g., $\cos(\frac{1}{2}kN + \frac{1}{2}\phi - kn)$=0). However, this is not a useful state because this also means that the output amplitude and hence the input amplitude of the fundamental frequency is zero at all the nodes. The zero input voltage at fundamental results in zero even harmonics at the output. An example of this condition can be viewed in Figure 1.2 at k=π.

The other way to cancel the odd harmonics is for any stage to cancel the odd harmonics of its adjacent stage. In this method, a total odd harmonic cancelation happens at the output only if the number of stages, N, is even. From (1.4a) we can derive the condition for cancelation of the fundamental component to be

$$\begin{aligned} &\cos(\frac{1}{2}kN + \frac{1}{2}\phi - kn) = -\cos(\frac{1}{2}kN + \frac{1}{2}\phi - k(n+1)) \\ \Rightarrow &k = \pi \quad OR \quad k(N-2n-1) + \phi = \pi. \end{aligned} \tag{1.5}$$

Two of the solutions for the above equation are k=π and k=0 which are not acceptable: k=0 means that the phase shift per section is zero and is impractical in Figure 1.1. k=π implies the 180° phase shift per section which occurs at the cut-off frequency of the line and again is not feasible. It is impossible to find an acceptable solution for all n's and all even N's. Therefore, we find the solutions of (1.5) for four different cases:

$$N = 2, 6, 10, ... \quad \& \quad n = even \Rightarrow \quad k = \pi/2 \quad \& \quad \phi = \pi/2, \tag{1.6a}$$

$$N = 2, 6, 10, ... \quad \& \quad n = odd \Rightarrow \quad k = \pi/2 \quad \& \quad \phi = 3\pi/2, \tag{1.6b}$$

$$N = 4, 8, 12, ... \quad \& \quad n = even \Rightarrow \quad k = \pi/2 \quad \& \quad \phi = 3\pi/2, \tag{1.6c}$$

$$N = 4, 8, 12, ... \quad \& \quad n = odd \Rightarrow \quad k = \pi/2 \quad \& \quad \phi = \pi/2. \tag{1.6d}$$

These are the conditions in which the fundamental component is canceled at the output of the multiplier. Similarly, it is easy to show that the same solutions in (1.6) will result in all the other odd harmonics to cancel out at the output. The solution of $k=\pi/2$ is practical to implement in Figure 1.1 and ensures that the center frequency is well below the cut-off of the line. If we have a 2-stage multiplier with $k=\phi=\pi/2$, based on (1.6a) the transistor at node n=0 (n=2,...) will cancel the odd harmonics of the transistor at node n=1 (n=3,...). That is why in Subsection 1.2.1 we chose $k=\phi$ and put the transistors at nodes n=0 and n=1 to perform the simulation. Figure 1.2 verifies that the odd harmonics are canceled at $k=\phi=\pi/2$.

1.2.3 Power Combining

Although the even harmonic components are in phase from different transistors, their amplitudes, as shown in (1.4), are a function of the node number, n, and may not be equal. The unequal harmonic amplitudes are the direct result of unequal standing wave amplitudes at the gate of the transistors. If we use the power combiner in Figure 1.1 the unequal even harmonic amplitudes result in an inefficient power combining. Therefore we need to design k and ϕ in order to have the same gate voltage amplitude for all the transistors. Using (1.4b), this translates to

$$\begin{aligned} &\cos(kN+\phi-2kn)=\cos(kN+\phi-2k(n+1)) \\ \Rightarrow &(kN+\phi-2kn)=\pm(kN+\phi-2k(n+1))+2m\pi, \end{aligned} \tag{1.7}$$

in which m is an integer. The solutions for (1.7) are derived to be

$$\begin{aligned} k &= m\pi, \\ \phi &= k(2n-N+1)+m\pi. \end{aligned} \tag{1.8}$$

The first solution can be expanded to two unique solutions of k=0 and $k=\pi$ which are not acceptable as discussed. The second solution may be acceptable but the problem is

that k and ϕ are a function of n which is variable. In order to have constant values for k and ϕ we expand the second solution for when N is even and odd:

$$\begin{aligned} N = even \Rightarrow \quad k = \pi/2 \quad \& \quad \phi = \pm\pi/2, \\ N = odd \Rightarrow \quad k = \pi/2 \quad \& \quad \phi = m\pi. \end{aligned} \tag{1.9}$$

These are the conditions in which the second harmonic components have the same amplitude from different transistors. Similarly, it is easy to show that the same solutions in (1.9) will result in all the other even harmonics to have the same amplitude from different transistors. Combining (1.6) and (1.9) we have the tools to design a multiplier using the topology in Figure 1.1.

It is noteworthy that as we move away from the center frequency in which (1.9) is satisfied, the power would not add up efficiently in Figure 1.1 and as a result the bandwidth drops compared to the simulation shown in Figure 1.2. However, the odd harmonic cancelation conditions in (1.6) are general and is valid for any kind of power combiner including the one shown in Figure 1.1.

Since the desired harmonics are in-phase at the output, a simple low-loss power combining network can be used to add the power. To ensure the same distance from each transistor to the load, a tree structure or a circular geometry can be used, as shown in Figure 1.3. This is a similar frequency multiplier as in Figure 1.1 with four sections. The only difference is that the inputs are connected together to make a single-input multiplier. The input signal is applied to the bottom of the structure and divides into two identical parallel paths and reflects back at point "A" which is the common-mode node for the input signal. The phase shift between the counter-propagating signals is designed to satisfy (1.6) and (1.9). The main advantage of the circular structure is that it enables us to realize the circuit using only one input that guarantees the frequency matching between the two traveling waves, as well as lower chip area. Furthermore, it

minimizes the length of the output power combiner, which means lower loss at the high output frequency.

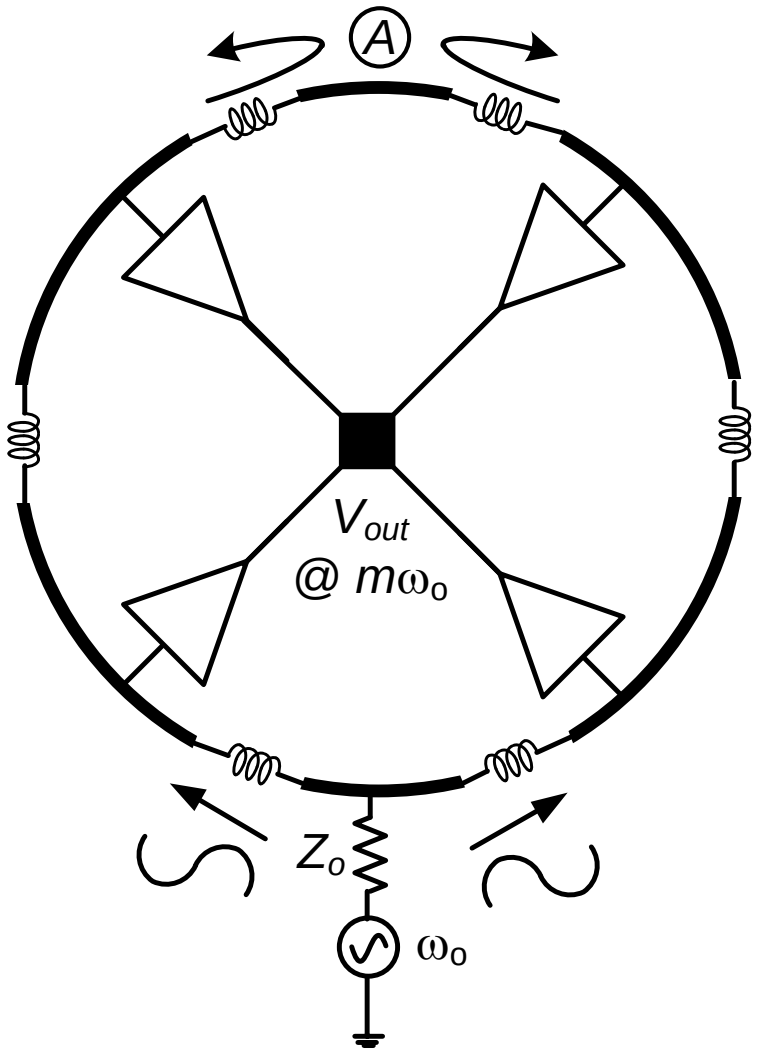


Figure 1.3: Circular geometry for the frequency multiplier.

1.3 A 220 GHz to 275 GHz Frequency Doubler

1.3.1 Design and Simulation

Figure 1.4 shows the CMOS implementation of the proposed frequency multiplier with four sections. The input matching network consists of C_{in} and L_{in} and the output matching network is constructed using L_d and C_d. As discussed, the incident wave travels from the signal source at the bottom of the structure and reflects back at point "A". To better illustrate the operation of the circuit in this example, the half circuit of the input network is shown in Figure 1.5. Assuming a good input matching, the voltages at different nodes are constructed by the superposition of the incident and reflected waves as shown in this figure. Here k is the wavenumber which is the phase shift per section and is defined by (1.2) and ϕ is the phase shift of the signal when it travels and reflects back through the last half-inductor, $L_g/2$. Due to zero phase shift of the signal at the end of this half inductor, ϕ is equal to k. Comparing the node voltages in Figure 1.5 with (1.1) it is verified that ϕ is the phase shift between the incident and reflected waves and the two transistors are at nodes n=0 and n=1. According to (1.6a) and (1.9) if we design the transmission line to have k=ϕ=$\pi/2$ at center frequency, we achieve effective even harmonic power combining and odd harmonic cancelation at the same time. The resulting second harmonic components at center frequency is shown at the output of the transistors in Figure 1.5.

A standard 65 nm CMOS process with a top metal thickness of 1.3 μm was used to implement the multiplier. The input frequency for this prototype is selected to be from 120 GHz to 150 GHz because of available measurement instruments for signal generation, coupling and detection. The second harmonic is selected at the output for higher power generation. Therefore the output matching network is designed to operate

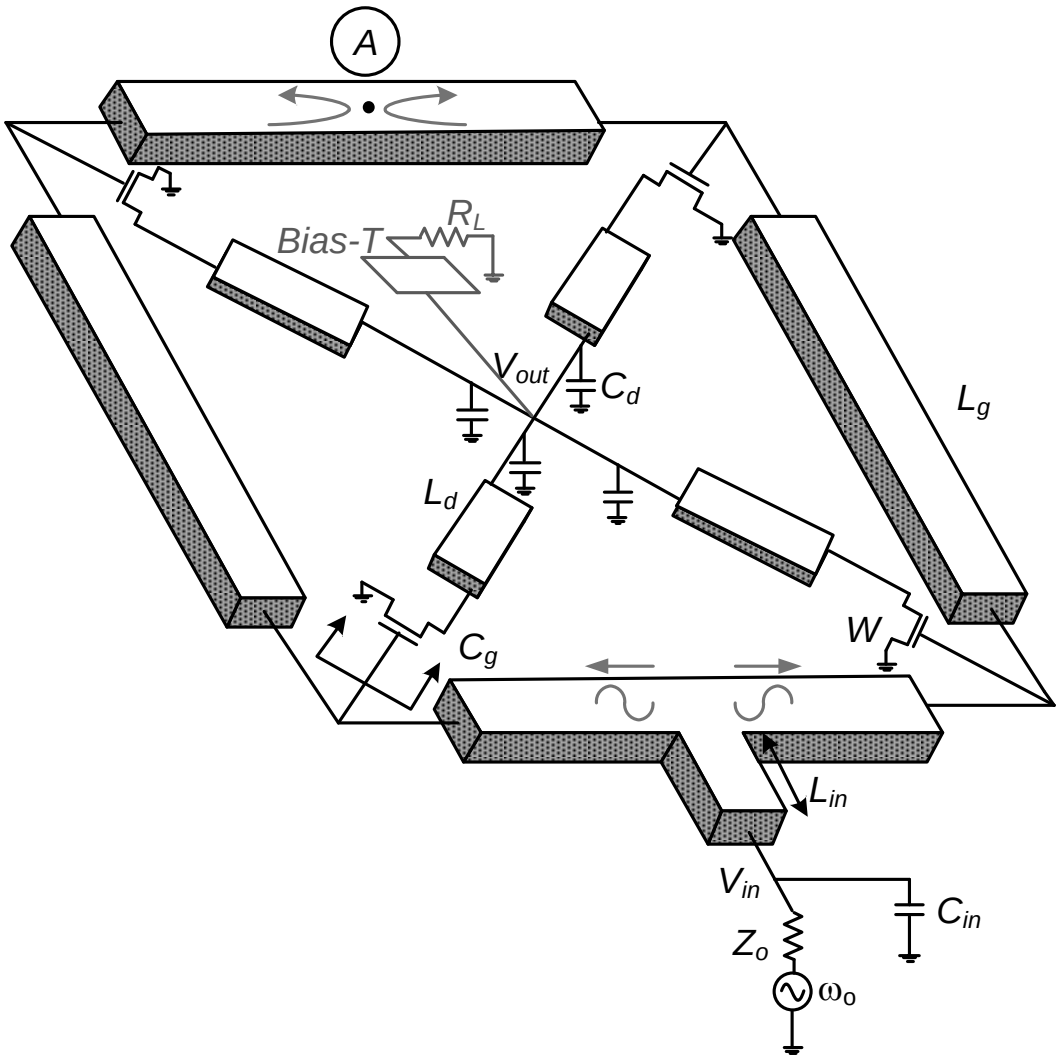


Figure 1.4: Circuit implementation of the proposed frequency multiplier.

from 240 GHz to 300 GHz. All the inductors and capacitors in this frequency doubler are realized using microstrip transmission lines and metal-to-metal capacitance of the probing pads, respectively. The Sonnet electromagnetic simulator was used to design all the passive components [30]. Since for strong harmonic generation high input power is applied to the doubler, the input matching should be designed for large signals. Figure 1.6 shows the simulated input reflection coefficient for an input power of 3 dBm. In this simulation L_g=60 pH is implemented using a microstrip transmission line with an

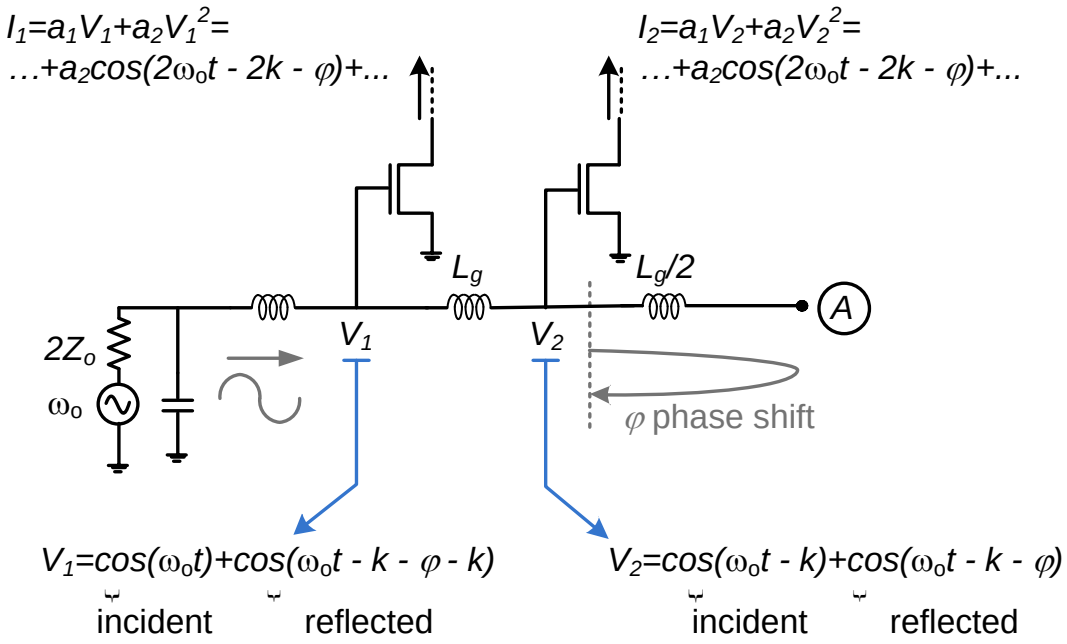


Figure 1.5: Half circuit of the input network of the frequency multiplier.

electrical length of $\lambda/5$ and quality factor of 13 at 135 GHz. This short electrical length enables us to use this transmission line as an inductor in the circuit. The transistor size of W=28 μm corresponding to C_g=55 fF are also used for this simulation. These component values result in $k \simeq \pi/2$ at the center frequency of 135 GHz. This k value along with ϕ=k which is a direct outcome of the topology satisfy the conditions in (1.6a) and (1.9). The L_g and C_g values are also designed to have good matching at the input.

The output impedance is matched to a 50 Ω load at $2\omega_\circ$ using L_d and C_d. Because the output matching network is matched at $2\omega_\circ$ it appears as an inductive load for the transistor at $\omega_\circ$. Under specific conditions the real impedance looking into the gate of a transistor with an inductive load is negative. This negative impedance can be used to cancel most of the loss of the input line, increasing the voltage swing at $\omega_\circ$ and hence creating significantly stronger harmonic power. Figure 1.7(a) shows the equivalent circuit of one section of the frequency doubler which can be used to find the gate input

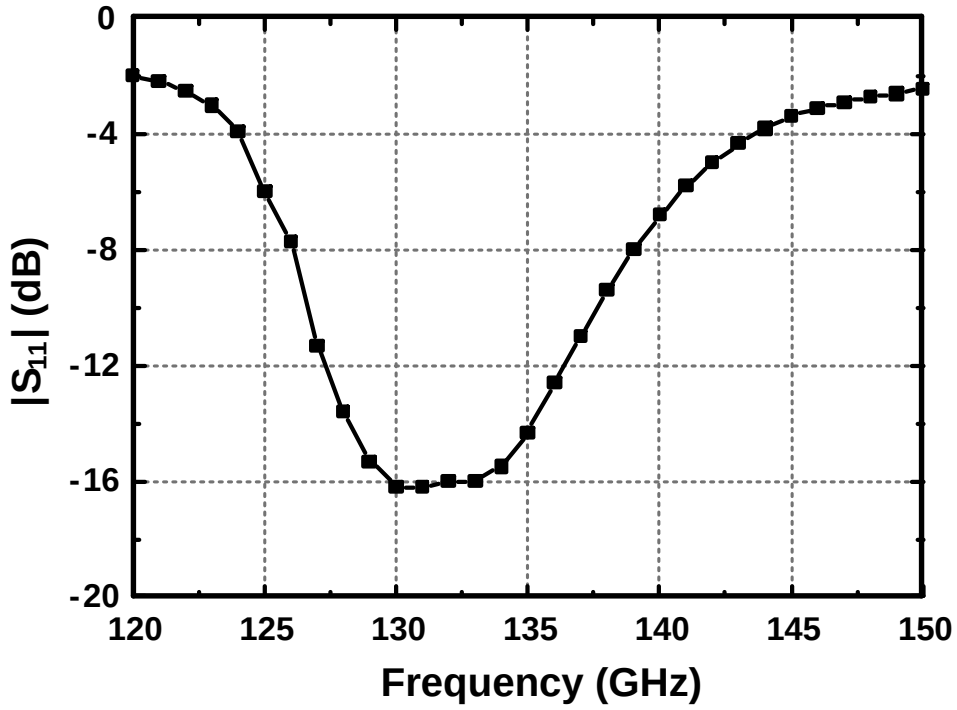


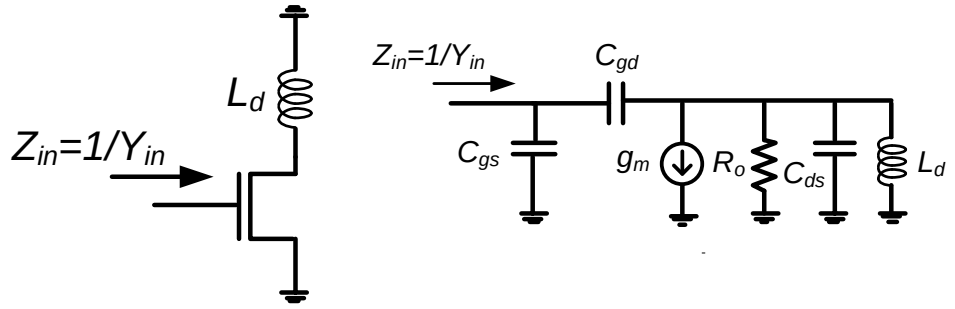
Figure 1.6: Simulated large-signal input reflection coefficient (S_{11}) of the frequency doubler.

impedance at $\omega_\circ$. Since the fundamental frequency is canceled out at the output, it is assumed to be grounded at this frequency. To find the condition for loss cancelation the real part of the input admittance is derived to be

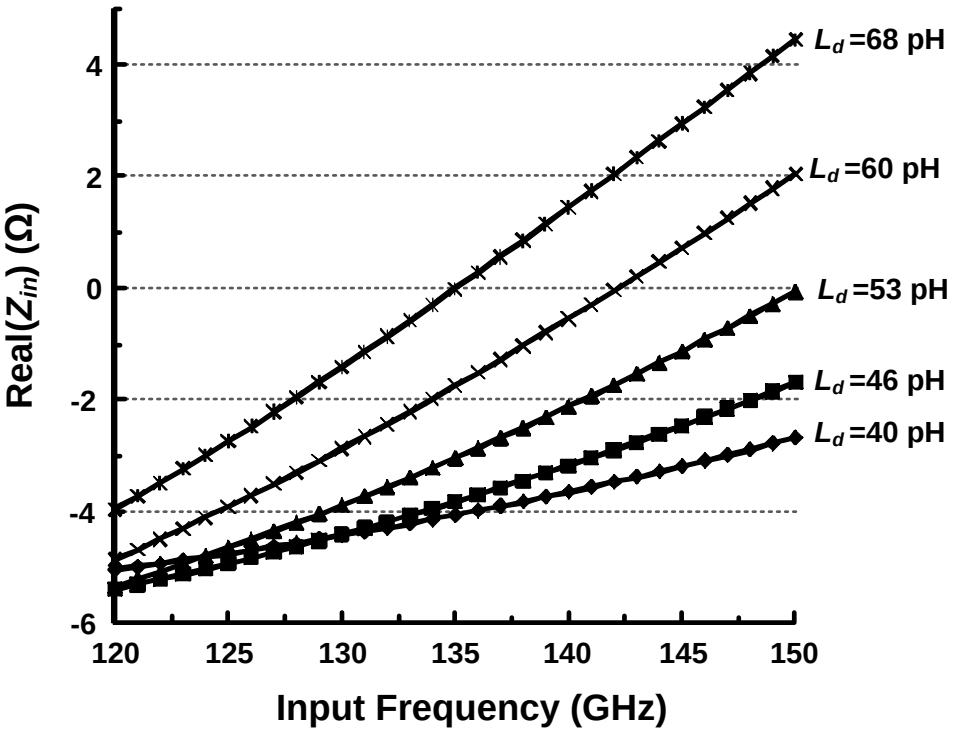
$$Real[Y_{in}] = \frac{\frac{C_{gd}g_m}{L_d}[L_d\omega_\circ^2(C_{gd} + C_{ds} + \frac{C_{gd}}{R_o g_m}) - 1]}{1/R_o^2 + [\omega_\circ(C_{gd} + C_{ds}) - \frac{1}{\omega_\circ L_d}]^2}, \tag{1.10}$$

where C_{gd} is the gate-drain capacitor, g_m is the transistor transconductance, and C_{ds} and R_o are the drain-source capacitor and resistor, respectively. Since the denominator in (1.10) is positive, the real part of the input impedance (or admittance) is negative if

$$L_d\omega_\circ^2(C_{gd} + C_{ds} + \frac{C_{gd}}{R_o g_m}) < 1. \tag{1.11}$$



(a)



(b)

Figure 1.7: (a) Equivalent circuit to find the input impedance at $\omega_\circ$ and (b) the simulated real part of the input impedance as a function of input frequency and L_d.

The gate resistance of the transistor is not included in deriving the input impedance. Therefore to get an actual negative resistance from the transistor the gate resistance should be compensated. To see the effect of all the losses in the transistor, the real input impedance is simulated as a function of input frequency and L_d in Figure 1.7(b). As verified by (1.10), Figure 1.7(b) shows that when the real part of the input impedance is around zero, lower frequency or lower L_d create a larger negative input resistance. There is a trade-off between harmonic matching at the output and loss cancelation at the input. Larger L_d creates a better output matching at the second harmonic but it also reduces the negative input impedance which in turn reduces the gate voltage swing and hence weaker harmonic generation. Optimum values for maximum output power are found to be L_d = 53 pH and C_d = 8 fF. These values are also selected to make the doubler unconditionally stable for all the frequencies above 80 GHz. Below 80 GHz the circuit is not unconditionally stable, however, it is stable with 50 Ω source and load impedances. At 270 GHz, the quality factor of L_d and C_d are 15 and 80, respectively. Figure 1.8 and Figure 1.9 show the doubler's simulated output reflection coefficient and stability factor (K-factor), respectively.

Figure 1.10 shows the simulated output power and conversion loss as a function of output frequency. In this simulation the input power is kept constant at 3 dBm at $\omega_\circ$. The peak output power and conversion gain occurs at 270 GHz. The simulated output power and conversion loss as a function of input power at the center frequency is plotted in Figure 1.11. A peak power of 1 dBm (1.3 mW) and a minimum conversion loss of 6 dB are achieved at this frequency. At the peak output power the doubler consumes 35 mW of DC power from a 1.2 V supply and input bias voltage is 1 V. Figure 1.12 demonstrates the simulated output spectrum when the input frequency and power are 135 GHz and 5 dBm, respectively. The power of all the other harmonics are at least 13 dB lower than the second harmonic at 270 GHz.

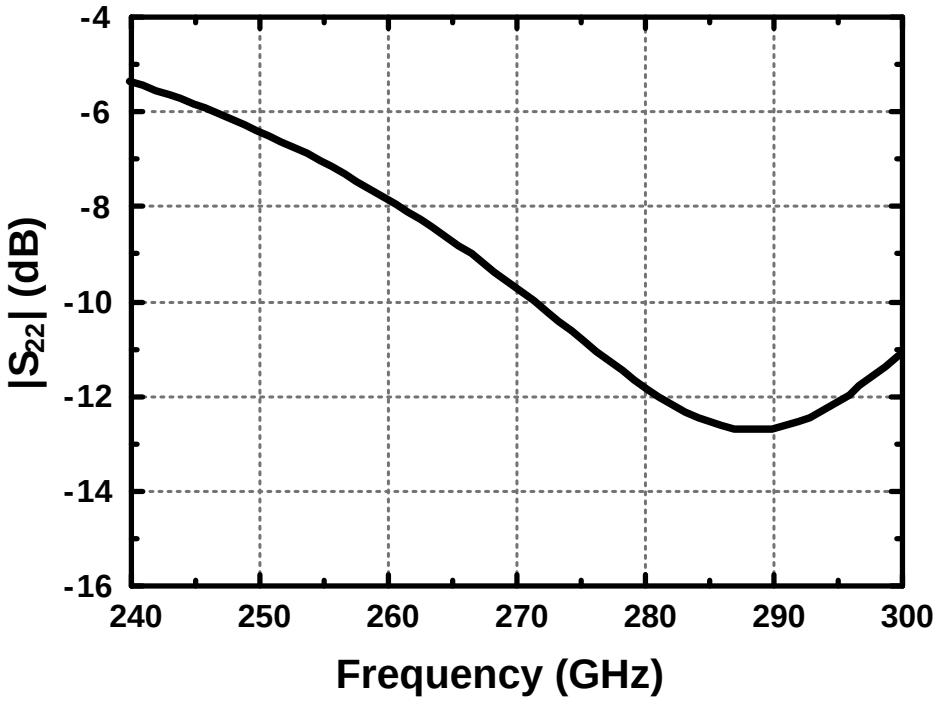


Figure 1.8: Simulated output reflection coefficient (S_{22}) of the frequency doubler.

1.3.2 Measurement

Figure 1.13 shows the die photo of the implemented frequency doubler. As discussed the input and output pads are part of the matching networks. To reduce substrate coupling the entire structure is shielded by a lower metal layer. This structure can be easily wire-bonded or flip chipped for external use. Furthermore, an antenna can be implemented at the center of the structure to radiate the power. If an on-chip integration with other blocks are required, a shielded line can be used to guide the signal from the center to the next block. A GGB 140-GSG probe and a Cascade i325-GSG probe with built-in bias tees were used to probe the input and output signals, respectively. The gate bias voltage and the DC supply are provided through the bias tees of the probes. The coupling between the probe and the on-chip transmission lines is minimized by the ground plane

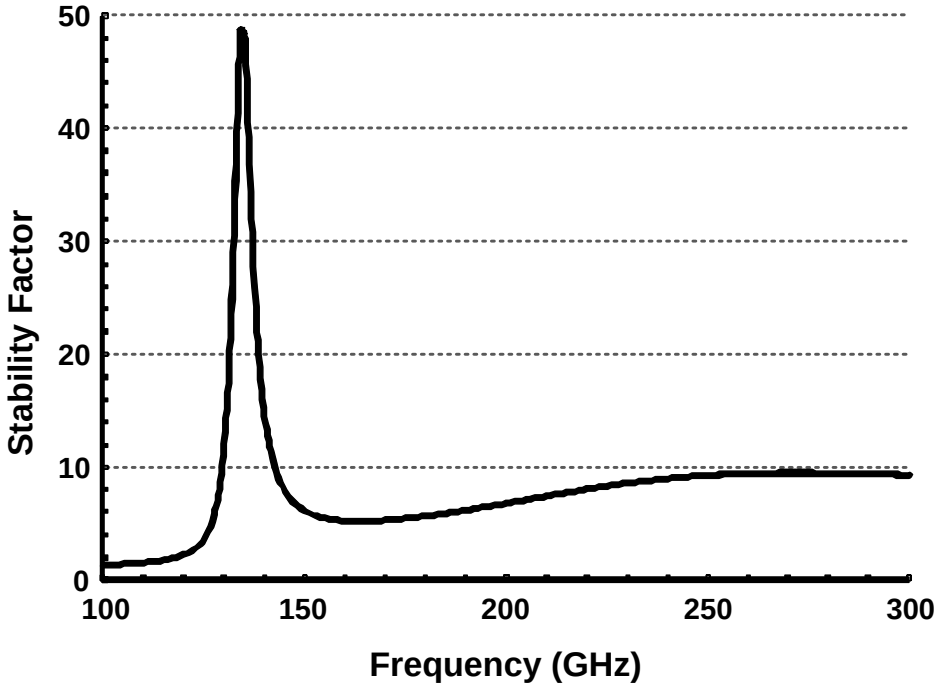


Figure 1.9: Stability factor (K-factor) of the frequency doubler as a function of frequency.

which is 6.9 μm away from the signal lines. As shown in Figure 1.14, two separate setups were used to measure the output frequency and power. Figure 1.14(a) shows the frequency measurement setup. A signal generator, an amplifier and a frequency tripler are used to generate the input signal. A harmonic mixer, an LO, and a spectrum analyzer are used to detect the output frequency. The output frequency measurement is limited to the range of 220 to 280GHz because of the lower and the higher cutoff frequency of the WR-3.0 and the WR-8.0 waveguides, respectively.

With no input signal, no signal was detected at the output or at the input. This means that the circuit is stable and no oscillation happens at the fundamental frequency and above. As the input power reaches -7.4 dBm the output power becomes detectable. By sweeping the LO frequency, f_{LO}, and observing the IF frequency which is $f_{IF}=f_{out}-nf_{LO}$, the LO harmonic number, n, and the signal frequency, f_{out}, can be determined [31]. The

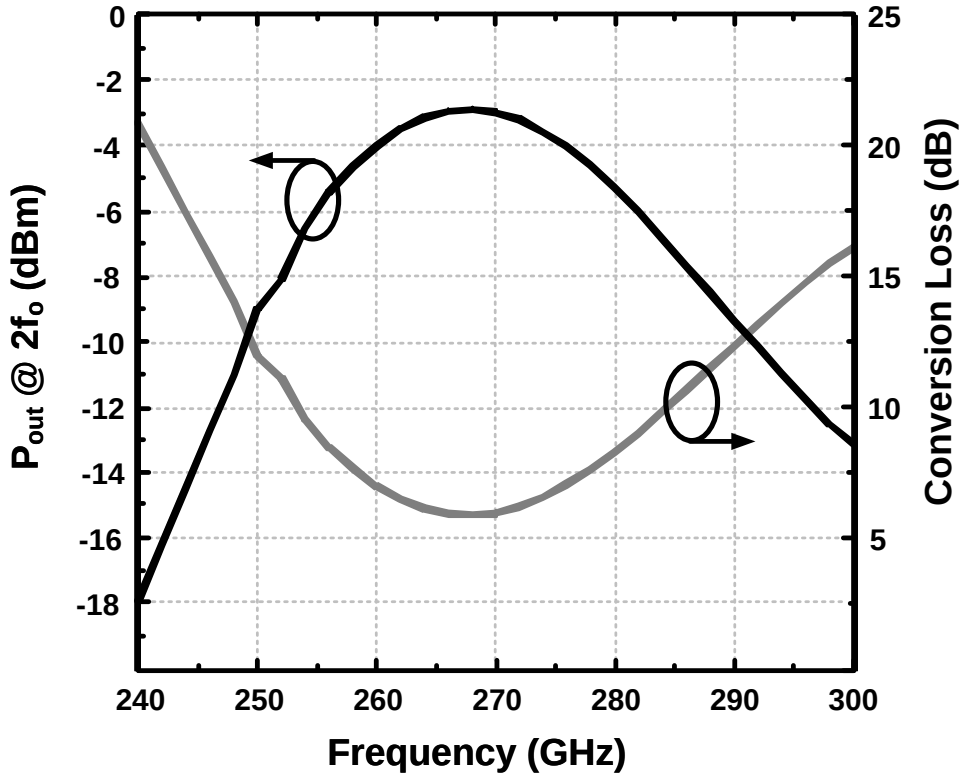


Figure 1.10: Simulated output power and conversion loss as a function of output frequency with a constant input power of 3 dBm.

detectable output signals from 220 GHz to 275 GHz were measured to have twice the frequencies of the input. A typical measured output spectrum with the 48th harmonic of the LO frequency is shown in Figure 1.15. For this spectrum, the input frequency and power are 118.5 GHz and 4.5 dBm, respectively. The loss of the probes and waveguides are characterized using network analyzer by Cascade and GGB and the output power of the VDI frequency tripler is measured using an Erickson PM4 power meter. Therefore, The input power of the implemented frequency doubler can be accurately characterized. Likewise, having the conversion loss of the OML harmonic mixer the output power of the frequency doubler can be estimated. For the 237 GHz signal in Figure 1.15 the loss of the output probe/waveguide and the conversion loss of the mixer for 48th harmonic of the LO frequency are 5 dB and 66 dB, respectively. Given the IF power of -71 dBm

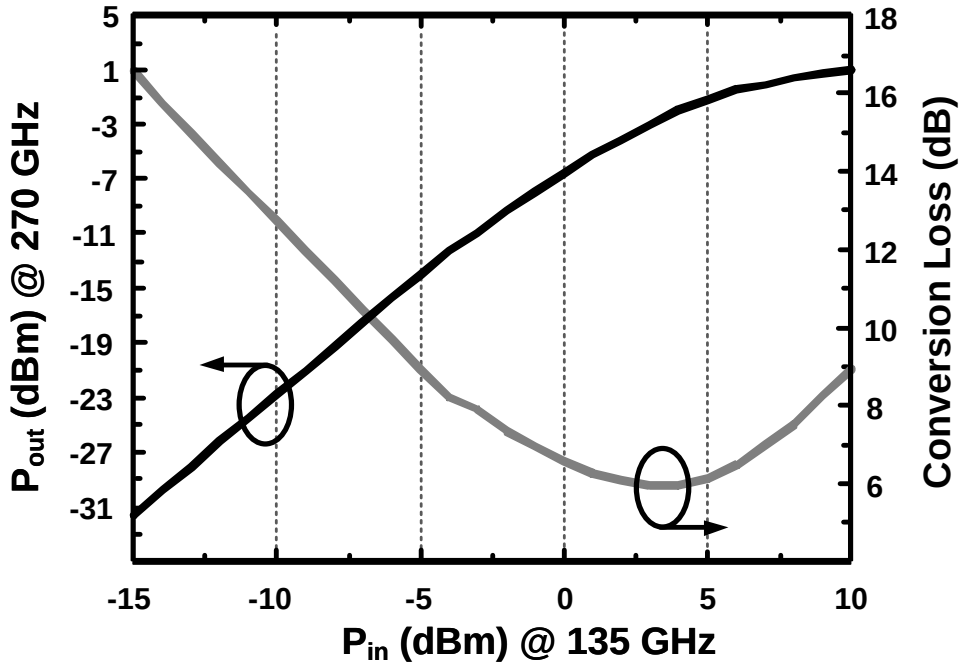


Figure 1.11: Simulated output power and conversion loss at 270 GHz as a function of input power.

the output power is 0 dBm at 237 GHz.

Although the output power can be estimated using harmonic mixers, it is not accurate. This is because harmonic mixers are highly nonlinear devices and it is almost impossible to characterize them for all power levels. To measure the output power accurately we use the setup in Figure 1.14(b) with an Erickson PM4 power meter at the output. The power meter works for all the frequencies from 75 GHz to 2 THz and its resolution is 10 nW. A WR-3.0 waveguide which has a pass-band from 220 GHz to 325 GHz is used to direct the signal to the power meter. As a result, all the harmonics below the second harmonic are highly suppressed before the signal reaches the power sensor. As shown in the simulation in Figure 1.12, all higher harmonics will either cancel out at the output, have low multiplication efficiency, or will be suppressed by the output matching network. This would result in the power meter readout to be mostly from the

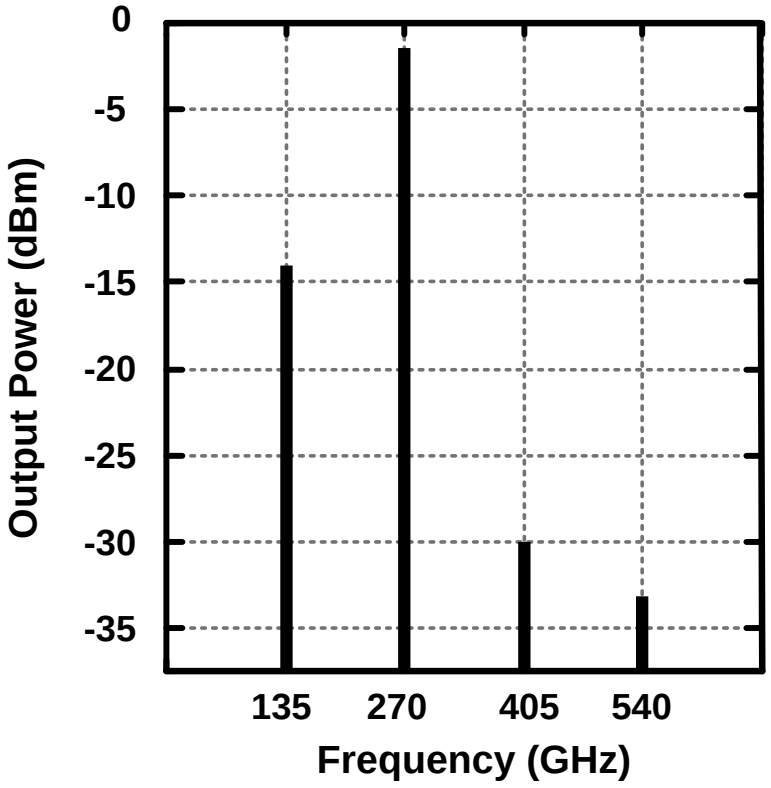


Figure 1.12: Simulation of a typical output spectrum when the input frequency and power are 135 GHz and 5 dBm respectively.

second harmonic component. A tapered waveguide is used to make a transition from WR-3.0 to WR-10 which is the wave guide dimension for the power sensor head.

Figure 1.16 shows the measured output power and conversion loss as a function of output frequency. In this measurement the input power is kept constant at 3 dBm for all frequencies. This input power level is the highest power that our setup can generate across the entire band. Using this input power, the frequency doubler operates from 220 GHz to 275 GHz. This operating range is limited to the lowest power that can be detected using our equipments. The 3-dB bandwidth of the doubler is from 234 GHz to 253 GHz. The power difference between this measurement and the one from the harmonic mixer is mostly because the mixer is calibrated at lower power levels and the

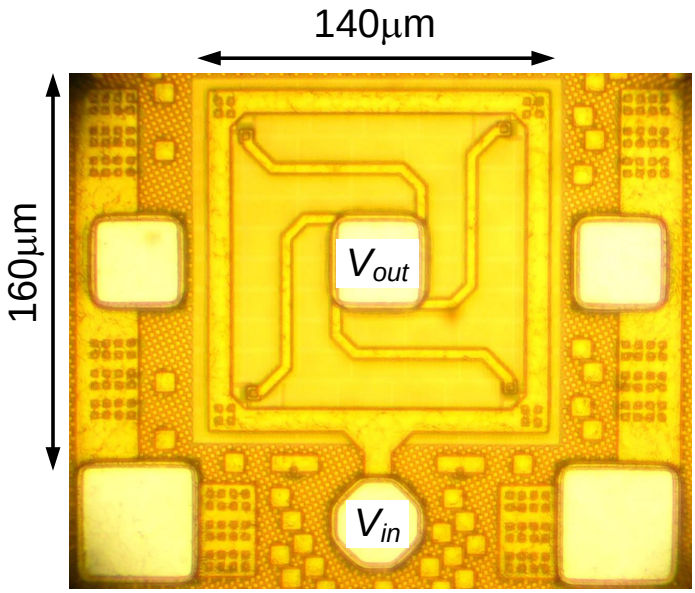
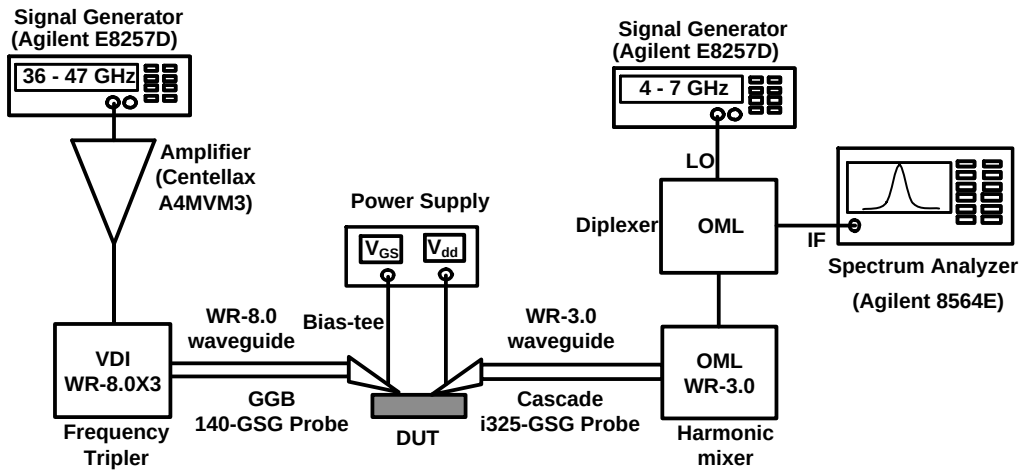


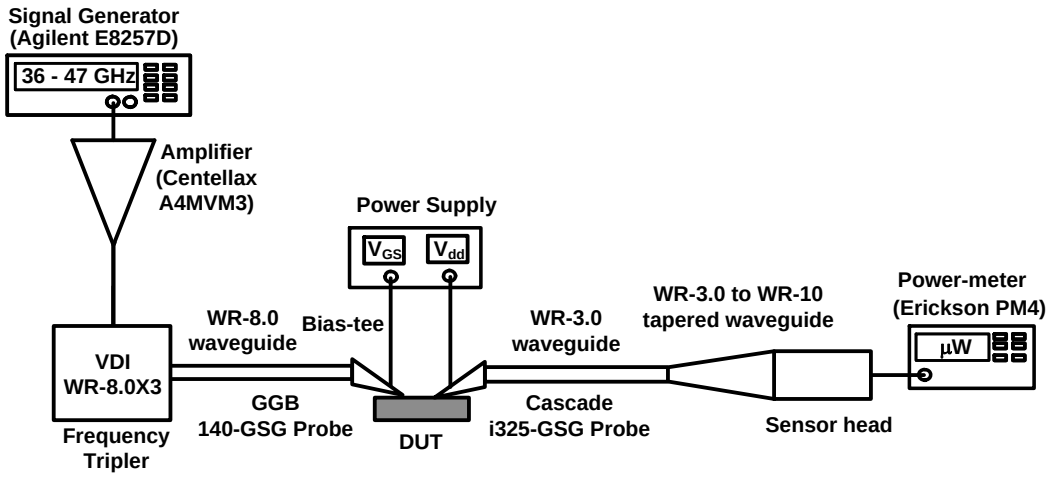
Figure 1.13: Die photo of the frequency doubler.

conversion loss values are not valid here. The peak measured power and conversion gain using this setup occurs at 244 GHz. The difference in output frequency range between the simulation and measurement is around 10%. This error is mostly caused by transistor parasitic modeling at this frequency range. Figure 1.17 shows the output power and conversion loss as a function of input power at 244 GHz. A peak output power of -6.6 dBm (220 μW) with a conversion loss of 11.4 dB is achieved at this frequency. The maximum input power that our setup can provide at 122 GHz is 4.8 dBm and therefore the output power is not saturated as shown in Figure 1.17. Given higher input power, we can achieve higher output power. Due to inaccurate modeling of the transistors the measured output power is around 3 dB lower than the simulation which is acceptable for this frequency range. The circuit consumes 40 mW of DC power from a 1.2 V supply.

The comparison with the state of the art is provided in Table 1.1. Compared to reported CMOS frequency multipliers this work has doubled both the operation fre-



(a)



(b)

Figure 1.14: Test setup for measuring (a) output frequency and (b) output power of the frequency doubler.

quency and tuning range at the same time. Although the output power is not saturated, it is higher than any other CMOS signal source at this frequency range. To have a fair comparison with other CMOS works, the output power is reported using both harmonic mixer and power meter. The doubler's specifications are comparable to monolithic compound semiconductor frequency multipliers.

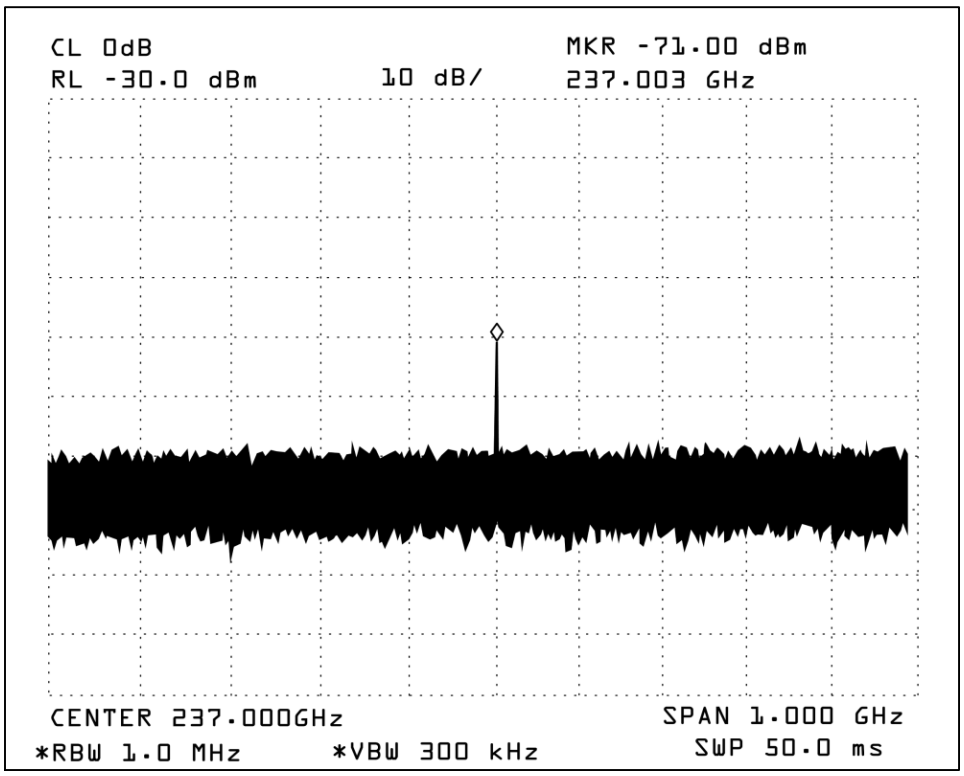


Figure 1.15: Measured output spectrum with the input power of 4.5 dBm at 118.5 GHz.

1.4 Conclusion

We have proposed a wideband frequency multiplier that effectively generates and combines harmonics from multiple transistors. The experimental results show considerable improvement in the output power and tuning range compared to the state of the art. The frequency multiplier can be used to replace varactor-based tunable sources in mm-wave and terahertz frequencies for imaging, spectroscopy, communication and radar systems.

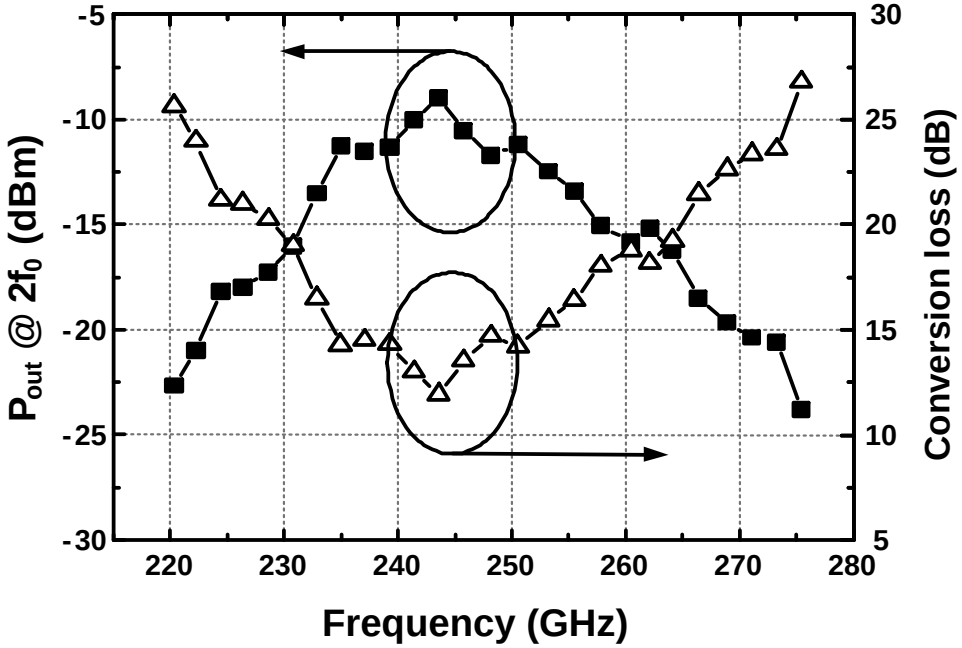


Figure 1.16: Measured output power and conversion loss as a function of output frequency using power meter for an input power of 3 dBm.

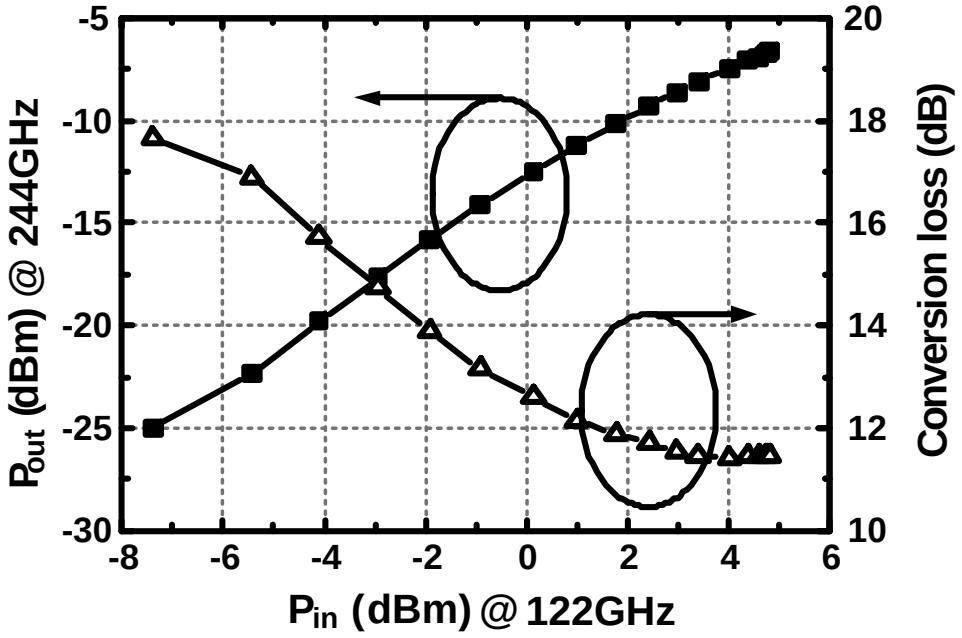


Figure 1.17: Measured output power and conversion loss as a function of input power at 244 GHz.

Table 1.1: Comparison with prior art

Ref.	This work	[9]	[14]	[26]	[32]	[3]	[24]	[21]	[12]
Frequency (GHz)	244	115	125	324	291	482	225	300	356
Tuning Range	22.2%	13.1%	12.7%	1.2%	NA	NA	17.7%	NA	11.7%
3-dB BW	7.8%	NA	NA	NA	NA	NA	11%	21.4%	9%
Power (dBm)	-6.6 / 0	-2.6	-1.5	-46	-17 (per element)	-7.9	-1	-6.4	8
Power Measurement	Power meter/ Mixer	Mixer	Mixer	Mixer	Mixer	Power meter	Power meter	Power meter	Power meter
Con. Loss (dB)	11.4	NA	10	NA	NA	NA	1	7.4	6.6
DC Power (mW)	40	12	0	12	18.7	61	630	NA	0
Monolithic Integration?	yes	yes	yes	yes	yes	yes	yes	yes	no
Type	×2 Traveling wave	×2 Injection locking	×2 Schottkey diode	Superposition VCO	Push-push Oscillator	Triple-Push Oscillator	×2 Push-push HBT	×2 Single transistor	×2 Schottkey diode
Technology	65 nm CMOS	65 nm CMOS	130 nm CMOS	90 nm CMOS	45 nm CMOS	65 nm CMOS	130 nm SiGe	50 nm GaAs mHEMT	GaAs Schottkey
Area (1000μm^2)	22.4	26.4	210	37.8	160	7.7	611	375	119

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CHAPTER 2

HIGH POWER TERAHERTZ AND mm-WAVE OSCILLATOR DESIGN: A SYSTEMATIC APPROACH

2.1 Introduction

There is growing interest in signal generation in the millimeter-wave and terahertz frequency ranges [1, 2]. There are numerous applications for mm-wave frequencies such as broadband wireless access (e.g., WiMax), vehicular radar, short-range communication, and ultra-narrow pulse generation for UWB radar [3,4]. Imaging and bio/molecular spectroscopy were the first and the main applications of the terahertz band, which is usually defined to be between 300 GHz and 3 THz [5–8]. Recently, this range has also been used for high data rate communication, compact range radar, and remote sensing [8–11].

Signal generation at these frequencies is a major challenge in solid-state electronics due to the limited cut-off frequency and breakdown voltage of active devices as well as the lower quality factor of passive components caused by ohmic and substrate loss. Traditionally, compound semiconductors are used to implement fundamental oscillators at mm-wave and terahertz frequencies [12–16]. Recently, SiGe and CMOS transistors were also employed to generate signals in the same frequency range using fundamental and push-push oscillators [17–26]. A fundamental oscillation frequency of 346 GHz is achieved in [13] using a 35 nm InP HEMT with a maximum oscillation frequency (f_{max}) of 600 GHz. SiGe HBTs with an f_{max} of 160 GHz are used in [24] to achieve a fundamental oscillation frequency of 100 GHz. A 104 GHz fundamental oscillator is also reported in [22], which employs 90 nm CMOS transistors with an f_{max} of 300 GHz. In all of these oscillators, the oscillation frequency is around half of the f_{max} of the transistors. The question that arises is whether the oscillators have exploited the full

capacity of the active devices in terms of output power and frequency. In other words, in any given process, it is essential to find the maximum oscillation frequency of a circuit topology, considering the quality factor of the passive components. Furthermore, for a fixed frequency, it is important to determine the topology that results in maximum output power.

In this paper, we address the above questions by investigating the effect of oscillator topology and the quality factor of the passive components on the oscillation frequency using the *activity condition* of the transistors [27]. We then introduce a methodology to design oscillators with frequencies close to the f_{max} of the transistors. Using this methodology in a 0.13 μm CMOS process with f_{max} of around 135 GHz [28], we design and implement 121 GHz and 104 GHz oscillators with the output power of -3.5 dBm and -2.7 dBm, respectively. Triple-push oscillators have been used to effectively generate third harmonics of the fundamental frequency [29, 30]. In this work, we introduce and realize a novel triple-push oscillator at 256 GHz with an output power of -17 dBm in the same 0.13 μm CMOS process. Next, using the same topology we implement a 482 GHz oscillator with a measured output power of -7.9 dBm in a 65 nm CMOS process. To the best of our knowledge, the 121 GHz and the 104 GHz oscillators have the highest power among CMOS oscillators in this frequency range, and the 121 GHz oscillator has the highest fundamental frequency in a 0.13 μm CMOS process. The 256 GHz oscillator has the highest frequency in a 0.13 μm CMOS process. The 482 GHz oscillator has the highest reported power in any CMOS or SiGe process and is comparable with InP HEMT and InP HBT in this frequency range.

The rest of this paper is organized as follows. In Section 2.2, the origin of f_{max} and the activity condition of a 2-port active device are discussed. In Section 2.3, we extend the theory of Section 2.2 for oscillators and use it to introduce a method for designing

high frequency oscillators. The design, simulation and measurement of the 121 GHz and 104 GHz oscillators are discussed in Section 2.4. The two triple-push oscillators at 256 GHz and 482 GHz, along with the simulation and measurement results are presented in Section 2.5. Finally, we summarize the paper in Section 2.6.

2.2 Overview of the Activity Condition of a 2-port Device

Activity condition determines the criterion in which the device can generate power. This is the basis for defining the maximum oscillation frequency, f_{max}. Before discussing the activity of a device, it is useful to understand Mason's invariant, U.

2.2.1 Unilateral Power Gain and the Origin of f_{max}

In 1954, Mason introduced the invariant function U for a linear 2-port network [31]. For a 3-terminal device as a linear 2-port network shown in Figure 2.1, U is defined as

$$U = \frac{|Y_{21} - Y_{12}|^2}{4(G_{11}G_{22} - G_{12}G_{21})}, \tag{2.1}$$

in which Y_{ij}'s are the elements of the admittance matrix of the network, $G_{ij} = Real[Y_{ij}]$, and $i, j = 1, 2$. The intriguing property of U is that it is invariant under any 4-port, linear, lossless, reciprocal embedding shown in Figure 2.2 [32]. The resulting embedded device is described by the admittance matrix, Y'. In other words for any 2-port device such as a transistor, U is only a function of the inherent characteristics of the device and not the embedding components. The fact that U is invariant under any linear, lossless, reciprocal embedding also implies that it does not change with respect to the node connections. For example, in a FET device, if we connect gate, source, and drain nodes to any of the three terminals of Figure 2.1, the value of U remains the same. Besides being invariant,

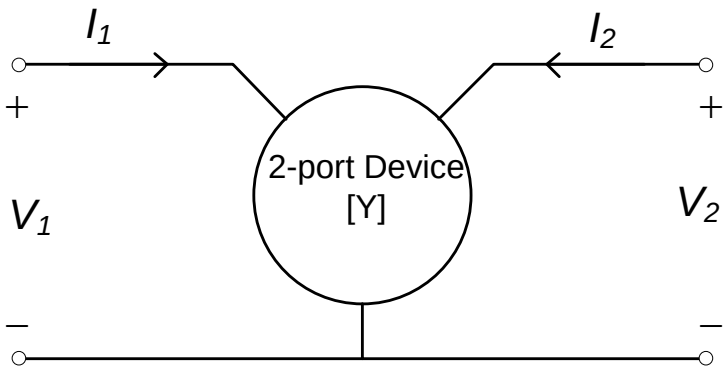


Figure 2.1: A 3-terminal 2-port device.

Mason showed that U is the maximum power gain when the reverse transmission in the embedded setting of Figure 2.2 is zero: $Y'_{12} = 0$ [31]. Thus, U is also called the unilateral power gain.

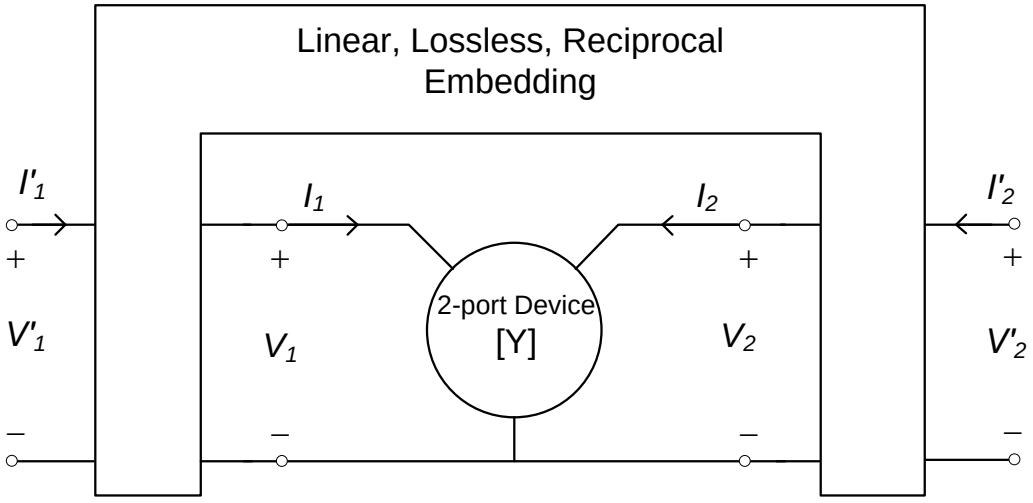


Figure 2.2: A device embedded in a 4-port, linear, lossless, reciprocal network.

In this paper, we are interested in the other property of U which is related to the activity of a device. A device is called active at a certain frequency if it can generate power in the form of single sinusoidal signal at that frequency [27]. It will be shown in

the next section that if $U > 1$, the device is active. Similar to other device characteristics, U is also a function of frequency and, in most cases, U decreases with frequency. The frequency that results in $U = 1$ is called the maximum oscillation frequency (f_{max}) [33]. Above this frequency, the device is not active, i.e., it cannot generate any power and hence no oscillation can be sustained. Note that f_{max} is also the frequency at which maximum available gain (G_{ma}) and maximum stable gain (G_{ms}) become unity [27]. Although G_{ma} and G_{ms} are often used to characterize the frequency response of a device, their shortcoming is that, unlike U, they change with the device embedding.

2.2.2 Activity Condition of 2-port Devices

To find the activity condition, first we find the real power flowing out of a device. For the device in Figure 2.1, we can write the total power going into the device as

$$P = V_1^* I_1 + V_2^* I_2, \tag{2.2}$$

in which "*" denotes the complex conjugate. Using the definition of the admittance matrix,

$$I_1 = Y_{11} V_1 + Y_{12} V_2$$
$$I_2 = Y_{21} V_1 + Y_{22} V_2,$$

we can rewrite (2.2) as

$$P = Y_{11}|V_1|^2 + Y_{22}|V_2|^2 + Y_{12} V_1^* V_2 + Y_{21} V_1 V_2^*. \tag{2.3}$$

Since we are interested in the sign of P, we can simplify (2.3) to

$$\frac{P}{|V_1||V_2|} = A^{-1} Y_{11} + A Y_{22} + Y_{12} e^{j\phi} + Y_{21} e^{-j\phi}, \tag{2.4}$$

in which

$$A = \frac{|V_2|}{|V_1|}, \quad \phi = \angle\frac{V_2}{V_1}. \tag{2.5}$$

From (2.4), the real power (P_R) that flows out of the device can be expressed as

$$\frac{P_R}{|V_1||V_2|} = -(A^{-1}G_{11} + AG_{22}) - |Y_{12} + Y_{21}^*|\cos(\angle(Y_{12} + Y_{21}^*) + \phi). \tag{2.6}$$

For the device to be active, the net power flowing out of the device should be positive, i.e. $P_R > 0$. Therefore, to find the limit of the device activity, we need to find the maximum of the right-hand side of (2.6). The maximization is in terms of A and ϕ which are the only parameters that are not a function of the device characteristics. There are two cases that we consider for this maximization: If G_{11} or G_{22} is negative, we can maximize the right-hand side of (2.6) by simply having a very low or very high A, respectively. This kind of activity is called *negative-conductance activity* and is rarely found in transistors [34]. This is because in most of today's semiconductor processes the stand-alone transistors exhibit positive input and output resistances for a wide range of frequencies. If G_{11} and G_{22} are positive, (2.6) is maximized by

$$A = A_{opt} = \sqrt{\frac{G_{11}}{G_{22}}} \tag{2.7}$$

and

$$\phi = \phi_{opt} = (2k + 1)\pi - \angle(Y_{12} + Y_{21}^*), \tag{2.8}$$

in which k is an arbitrary integer. By substituting (2.7) and (2.8) into (2.6), we arrive at

$$max(\frac{P_R}{|V_1||V_2|}) = -2\sqrt{G_{11}G_{22}} + |Y_{12} + Y_{21}^*|. \tag{2.9}$$

For the device to be active, (2.9) should be positive, which means that the activity condition of the device in Figure 2.1 can be written as

$$4G_{11}G_{22} < |Y_{12} + Y_{21}^*|^2. \tag{2.10}$$

This kind of activity is called *transfer activity* and is of particular importance for transistors. Using (2.1), it can be shown that the condition in (2.10) is equivalent to [32]

$$U > 1. \tag{2.11}$$

This is the reason U is used to determine if a device is active at a specific frequency.

As discussed in Section 2.2.1, f_{max} is the frequency at which U becomes unity. However, based on the above discussion the only way to satisfy the activity condition of (2.10) and have an oscillator at f_{max} is for A and ϕ to meet the optimal conditions of (2.7) and (2.8). Note that A and ϕ describe the relation between the voltage amplitude and phase of the two ports of the transistor and for a given oscillator topology, they are usually constant. As a result, the maximum frequency of oscillation in a fixed topology can be significantly lower than the device limit. For example in a cross-coupled oscillator the phase difference between gate and drain voltages is set to 180°. If the ϕ_{opt} in (2.8) is not 180°, then it is impossible to reach an oscillation frequency of f_{max}, even if we use ideal inductors and capacitors.

2.3 Activity Condition and Oscillator Design

In this section we expand the theory of activity condition to design oscillators with operation frequencies close to the f_{max} of the active devices. First, we find the maximum frequency of multi-stage ring structures. Note that the popular cross-coupled oscillator is a special case of the ring oscillator with two stages. After that, we present a method to design an oscillator that exploits the full capacity of transistors to achieve the maximum frequency in any given process.

2.3.1 Maximum Frequency of Ring Oscillators

Consider an N-stage ring oscillator with inductive loading as shown in Figure 2.3. We

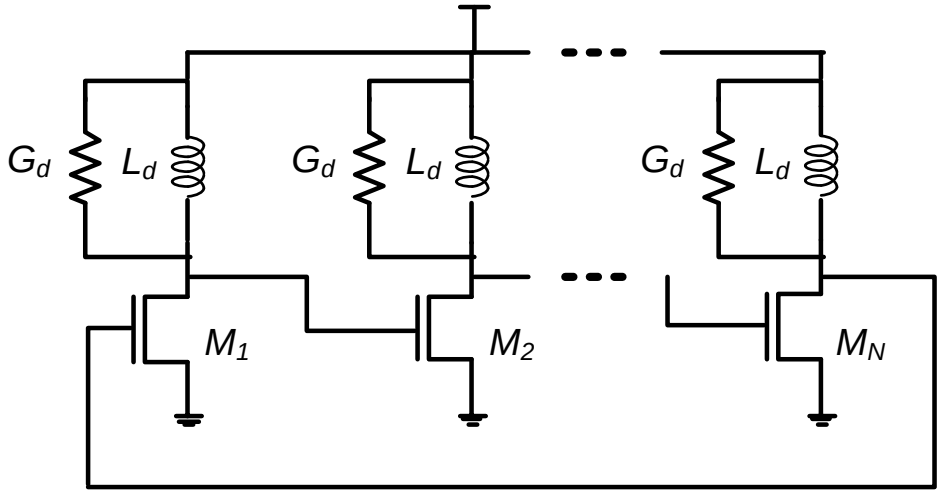


Figure 2.3: An N-stage ring oscillator with inductive loading.

use inductive loads instead of resistive loads to reduce the power loss and hence increase the maximum frequency of the oscillator [35]. Even though Figure 2.3 shows an oscillator with CMOS transistors, the analysis is valid for any 3-terminal device. Figure 2.4(a) shows a stand-alone transistor and Figure 2.4(b) shows a transistor inside the ring structure. It can be readily seen that the latter has additional conditions on the voltage gain and phase shift compared to the former. Since the goal is to find the maximum oscillation frequency, we can assume that the oscillator operates close to its limit and hence the voltage swing is not large, even at steady-state. This enables us to use small-signal Y parameters. If the voltage swing is not small, as we will discuss in Section 2.3.2, large-signal Y parameters should be used. With this in mind, we can find the voltage gain and phase shift for each section of the ring to be

$$A' = \frac{|V_2'|}{|V_1'|} = 1, \quad \phi' = \angle\frac{V_2'}{V_1'} = k\frac{2\pi}{N}, \tag{2.12}$$

in which k is an integer number. Combining (2.6), (2.12), and Y parameters of both networks in Figure 2.4, we can write the activity condition of the 2-port network in Figure 2.4(b) to be

$$G_m = \frac{P'_R}{|V'_1||V'_2|} = -(G_{11} + G_{22} + G_d) - |Y_{12} + Y_{21}^*| \cos(\angle(Y_{12} + Y_{21}^*) + k\frac{2\pi}{N}) > 0, \quad (2.13)$$

where P'_R is the real power flowing out of the device inside the ring and G_d is the parallel conductance of the inductor. It is interesting that the value of the inductors does not directly appear in (2.13). The activity condition is only a function of G_d and Y parameters of the stand-alone transistor.

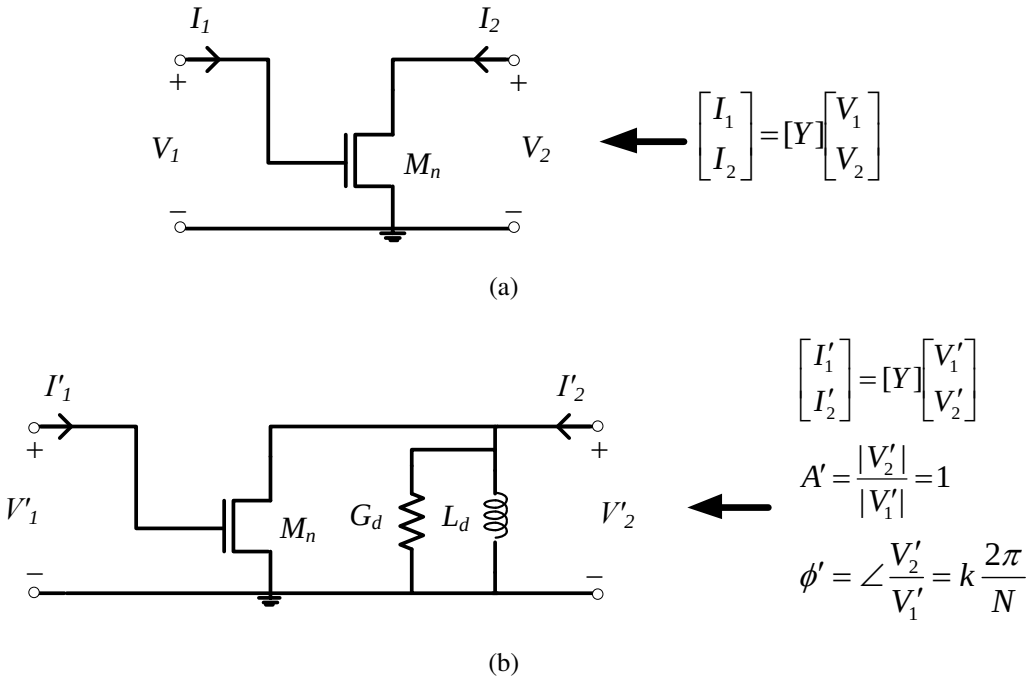


Figure 2.4: (a) A stand-alone transistor and (b) a transistor inside a ring oscillator with inductive loading.

The maximum frequency at which (2.13) is satisfied is the maximum frequency of oscillation for a ring oscillator with N stages. We call this frequency f_{m-N}. It also results from (2.13) that at a specific frequency, G_m is the maximum conductance (e.g., maxi-

mum G_d) that can be placed across the transistor ports and still sustain the oscillation. If G_d is positive, (2.13) shows that f_{m-N} is less than the f_{max} of the transistor. Even if $G_d = 0$, f_{m-N} may be less than f_{max} because the conditions of (2.12) may not be the same as the conditions of (2.7) and (2.8). As an example, we find f_{m-N} for a cross-coupled oscillator ($N = 2$) and a 3-stage ring oscillator ($N = 3$) in a 0.13 μm CMOS process:

Cross-Coupled Oscillator For $N = 2$ there are two distinct modes: $k = 0$ and $k = 1$. These correspond to the phase shift of $\phi' = 0^\circ$ and $\phi' = 180^\circ$ per section. Here, each oscillation "mode" represents a different phase shift per section that can exist in a ring structure in steady state. Figure 2.5 shows the plot of G_m for these two modes using a transistor width of 10 μm with 10 fingers in a common source configuration. The power consumption is 11 mW with power supply and gate-source voltage of $V_{dd} = V_{gs} = 1.5$ V. Figure 2.5 shows that no power can flow out of transistor for the mode $\phi' = 0^\circ$ and hence no oscillation would be sustained in that mode. Intuitively this is because in this mode, the current and voltage of the drain are in phase and hence the power that flows into the drain is positive, which means the device is equivalent to a passive component. In the second mode ($\phi' = 180^\circ$) with $G_d = 0$, the oscillator can oscillate through the maximum frequency of oscillation of $f_{m-2} = 120.7$ GHz. The f_{max} of the transistor is 174 GHz and is much higher than f_{m-2}. This proves that even though $G_d = 0$, maximum frequency of oscillation in a cross-coupled oscillator can not reach the f_{max} of the transistor in this process. A time domain simulation of a cross-coupled oscillator with $G_d = 0$ verifies the fact that the oscillation frequency cannot exceed 120.7 GHz. In a real circuit, G_d is non-zero and we need to back off from f_{m-2} to have an oscillation. For example Figure 2.5 shows that to oscillate at 100 GHz, the inductors can have a maximum G_d of 1.5 mS. As will be discussed in the next section, this will put a limit on the inductor quality factor.

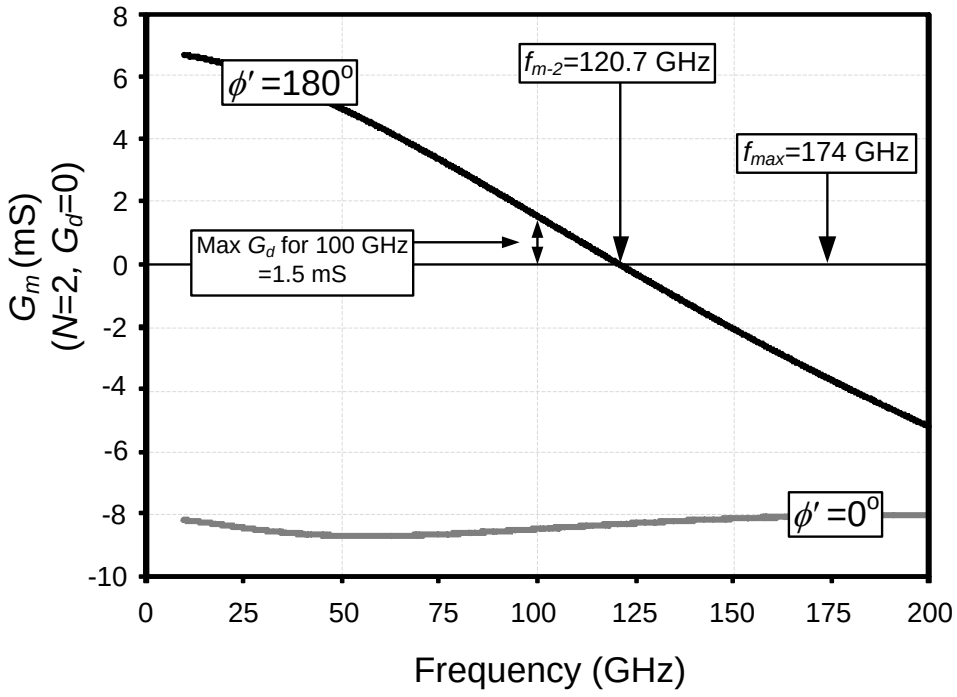


Figure 2.5: Simulation of G_m and the maximum frequency of oscillation (f_{m-2}) for a cross-coupled oscillator (2-stage ring oscillator) in the employed 0.13 μm CMOS process.

3-Stage Ring Oscillator Figure 2.6 shows G_m for three distinct modes of a 3-stage ring oscillator. The same biasing conditions as in Figure 2.5 are used in this graph. Here, similar to the cross-coupled oscillator the mode of $\phi' = 0°$ cannot sustain oscillation. The mode $\phi' = -120°$ only results in oscillation for frequencies below 40 GHz. The maximum frequency of oscillation happens for the mode $\phi' = 120°$. f_{m-3} is 172 GHz and is very close to the f_{max} of the transistors. This is because $\phi' = 120°$ is very close to the condition of (2.8), which for this process is $\phi' \simeq 112°$. A time domain simulation of a 3-stage ring oscillator with $G_d = 0$ verifies that the oscillation frequency can actually reach 172 GHz. As shown in Figure 2.6, the maximum G_d for 100 GHz oscillation is 3 mS and is twice the maximum G_d in the cross-coupled oscillator at the same frequency. Furthermore, if both structures oscillate at 100 GHz, the inductors used in the cross-

coupled oscillator should be smaller to provide the right phase shift. This leads to higher G_d for the cross-coupled oscillator, given that the inductor quality factors are the same. As it will be discussed in the next section, in this process, the 3-stage oscillator will result in a higher voltage swing in almost all frequencies because of the higher G_m as well as lower inductor G_d value for the same frequency.

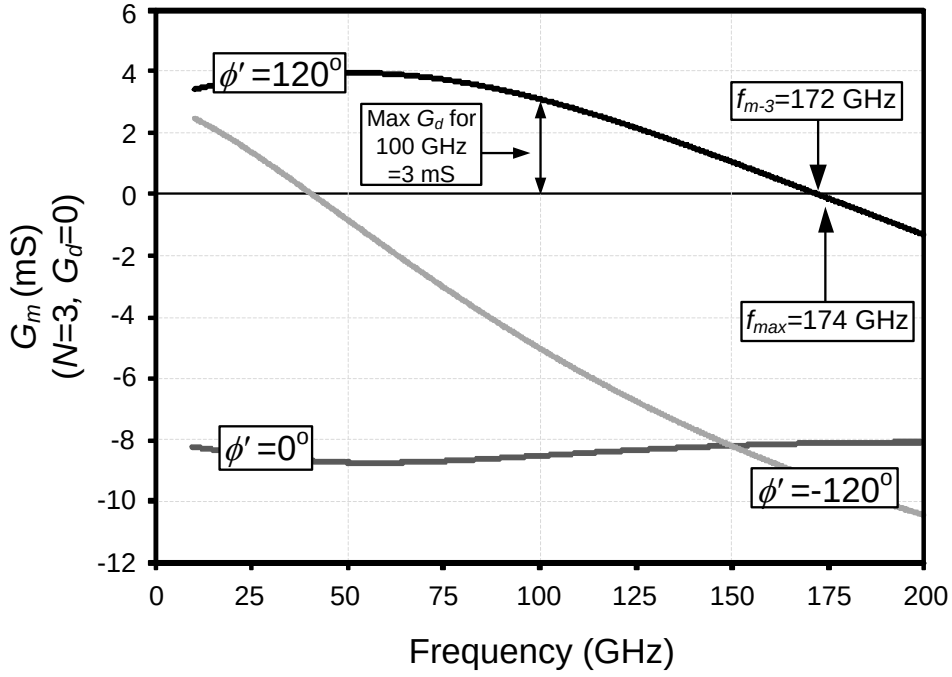


Figure 2.6: Simulation of G_m and the maximum frequency of oscillation (f_{m-3}) for a 3-stage ring oscillator in the employed 0.13 μm CMOS process.

The same procedure can be applied to any ring oscillator with a phase shift per section of ϕ' to find the maximum frequency of oscillation, f_m. Figure 2.7 shows the plot of f_m as a function of ϕ' for the employed CMOS process. Different ϕ' can be achieved by using different number of stages in a ring structure. As examples, the points associated with N=2 and N=3 is annotated in the figure. For other oscillator topologies it is possible to derive voltage amplitude and phase conditions similar to (2.12) in order to find the maximum frequency of oscillation, f_m. In Section 2.3.3 we discuss a methodology

to design oscillators that oscillate at frequencies close to the f_{max} of the transistors.

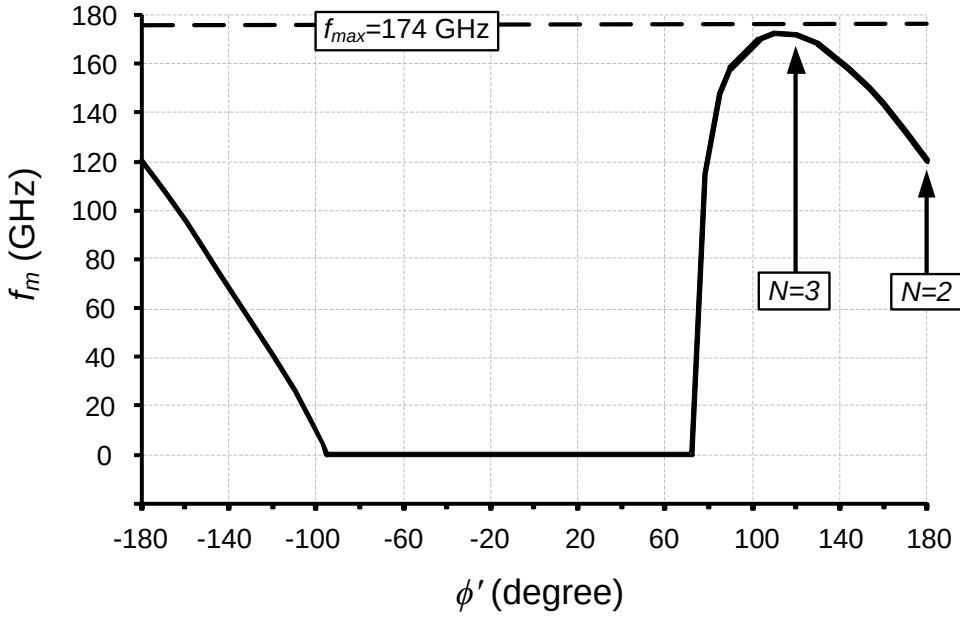


Figure 2.7: Simulation of the maximum frequency of oscillation (f_m) of a ring oscillator as a function of phase shift per section (ϕ') in the employed 0.13 μm CMOS process.

2.3.2 Voltage Swing of Ring Oscillators

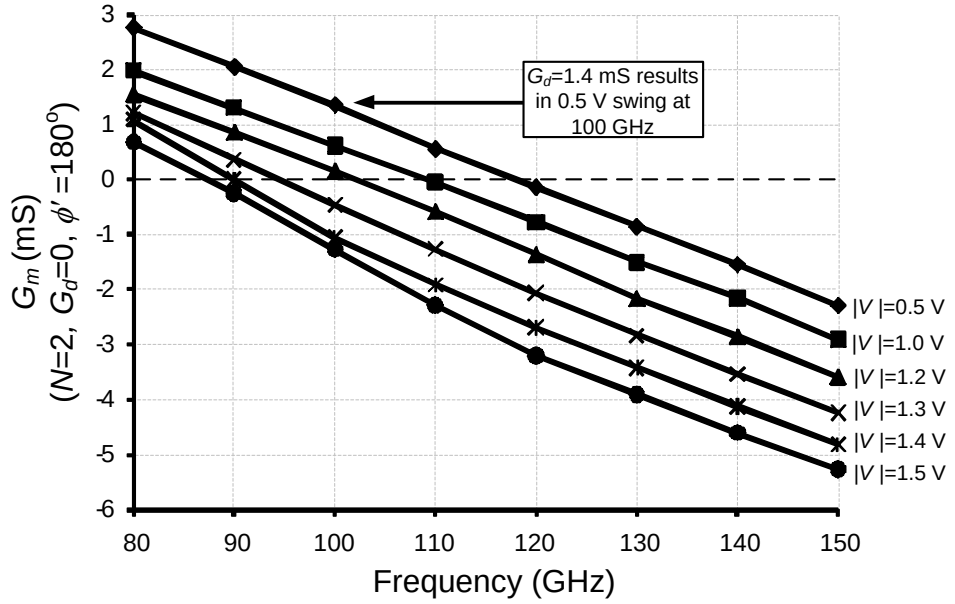
The large-signal dynamics of the ring oscillators can also be explained by using the large-signal Y parameters in the activity condition of (2.13). P'_R is the real power flowing out of one section of the oscillator and it should be zero at the steady state oscillation. This means that in the steady state, the generated power by the transistor is equal to the power lost in the transistor and the inductor (e.g., G_d). If the small-signal P'_R is positive at a certain frequency, the oscillation is possible at that frequency. This is the start-up condition and it leads to an increase in the voltage swing (e.g., $|V|=|V'_1|=|V'_2|$) of the section in Figure 2.4(b). As the voltage amplitude increases, the Y parameters of the

transistor also changes to the extent that P'_R or G_m in (2.13) becomes zero. At this point the voltage amplitude stays constant and an steady state oscillation is reached. As an example, Figure 2.8 shows the simulated large-signal G_m for 2- and 3-stage ring oscillators in the same 0.13 μm CMOS process. The Y parameters of the section in Figure 2.4(b) is simulated for different voltage amplitudes, $|V|=|V'_1|=|V'_2|$, and are inserted in (2.13) to find G_m of Figure 2.8. As the voltage amplitude increases, the G_m curve starts to move down until it crosses the zero line at the oscillation frequency. For example if both 2- and 3-stage oscillators are set to oscillate at 100 GHz using ideal inductors, Figure 2.8 shows that the 2- and 3-stage oscillators will have a voltage swing of around 1.2 V and 1.5 V, respectively. A time domain oscillator simulation verifies the exact predicted voltage swings for both oscillators.

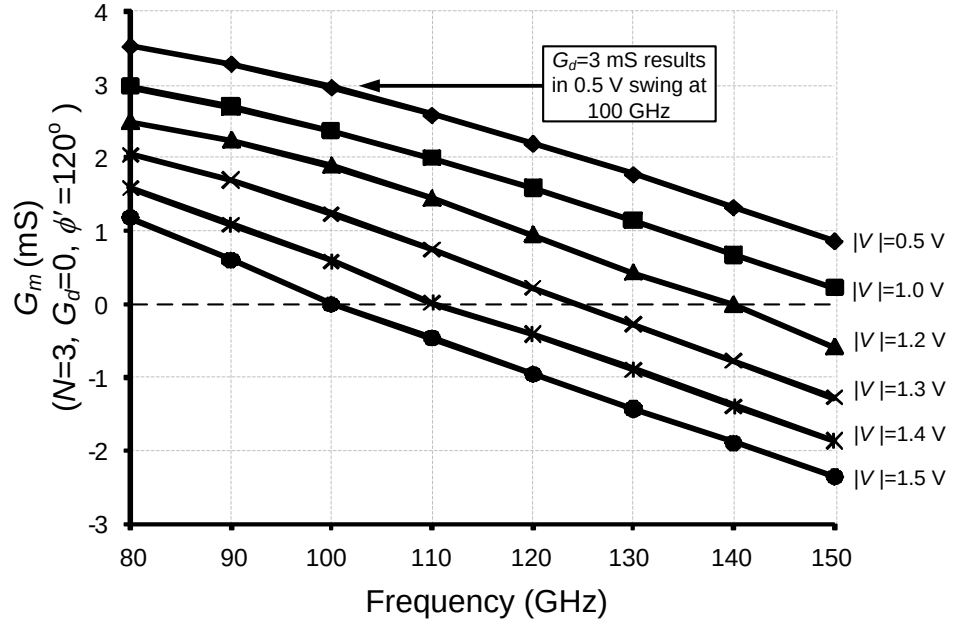
Repeating the same example for different frequencies shows that the 3-stage oscillator results in higher voltage swing than the 2-stage structure. This is because the starting small-signal G_m value is lower for the 2-stage ring (as we saw in Section 2.3.1) and the G_m curve variation for different voltage amplitudes are almost the same for both oscillators. Since G_d is a linear conductance associated with the inductor, it can be linearly subtracted from the curves in Figure 2.8 to find the voltage swings. For example in the 2- and 3-stage rings, a voltage swing of 0.5 V can be achieved at 100 GHz if the G_d of 1.4 mS and 3 mS is used, respectively.

2.3.3 Design Methodology of High-Frequency Fundamental Oscillators

Higher order harmonic oscillators with frequencies close to and beyond the f_{max} of the transistors have been reported [20, 36, 37]. However, most of these designs use push-



(a)



(b)

Figure 2.8: Simulated large-signal G_m as a function of different voltage amplitudes ($|V|=|V_1'|=|V_2'|$) in (a) 2-stage and (b) 3-stage ring oscillators.

push structures to utilize the second harmonic of the fundamental oscillation frequency. This results in low output power and hence fundamental oscillators are more desirable for high power generation. Using the theory discussed in the previous sections, we introduce a method to take full advantage of the transistor capabilities to design high-frequency fundamental oscillators. Here is the design methodology:

1. *Find the f_{max} of the process*: This can be done by measurement or simulation. In the case of simulation, it is noteworthy that because f_{max} is often obtained from extrapolation, it is usually higher than the actual value [22]. Also, f_{max} is layout dependent, so the same layout that was used in finding f_{max} should be used in the rest of the design process. Finally, to maximize f_{max}, we need to use multiple fingers and avoid a large transistor width [22].

2. *Choose an oscillation frequency (f_{osc}) below f_{max}*: That is if an oscillation frequency is desired. If the objective is to maximize the frequency, we pick an initial value and if, in the next steps, we find that the passive components are good enough, we come back to increase the frequency.

3. *Find A_{opt} and ϕ_{opt} at f_{osc} using (2.7) and (2.8)*: If these conditions are met, the maximum conductance (G_d) can be placed at the transistor ports at f_{osc}. Since simulation shows that (2.7) and (2.8) are not strong functions of the transistor width, the same transistor used in step 1 can be used here.

4. *Find an oscillator topology that satisfies the A_{opt} and ϕ_{opt} values*: These values can be satisfied by the inherent characteristics of the topology, e.g., in a ring oscillator, or by tuning the passive components of the oscillator, e.g., in Colpitts oscillator. Sometimes it is hard to achieve the exact values of A_{opt} and ϕ_{opt}, but it still boosts the frequency if A and ϕ are close to the optimum values.

5. *Choose the transistor width and passive component values*: This part can be done

using ideal passive components. Based on the chosen topology, f_{osc}, and the power budget, we can find the component values and sizes. Usually another restriction exists for the sizes of the transistor and passive components. If the transistor is too large, the corresponding inductor/capacitor size becomes too small and comparable with the parasitics, making it hard to design and control, specially at high f_{osc}. After choosing the transistor size we need to find its f_{max} and make sure it is still higher than f_{osc}. If not, we need to go back to step 2 and reduce the f_{osc}.

6. *Find the maximum conductances that can be placed at the transistor ports at f_{osc}*: Having the topology and the component values, we can find the actual A and ϕ that can be slightly different than A_{opt} and ϕ_{opt}. For example, in ring oscillators the maximum conductance, G_d, can be found using $A = 1$, $\phi = k2\pi/N$, and (2.13). We can model most of the other oscillators as an active device embedded in a passive network, as shown in Figure 2.9. Here G_{11}^p and G_{22}^p represent the loss of termination at the input and output of the transistor. The maximum conductances that can sustain the oscillation are the maximum G_{11}^p and G_{22}^p and their ranges can be found using

$$(A^{-1}(G_{11} + G_{11}^p) + A(G_{22} + G_{22}^p)) + |Y_{12} + Y_{21}^*| \cos(\angle(Y_{12} + Y_{21}^*) + \phi) < 0, \quad (2.14)$$

which was derived from (2.6).

7. *Design the passive components to satisfy (2.14)*: In this step, we replace the ideal passive components with real ones. Since we know their values from step 5, we only need to maximize their quality factor, e.g., by using E/M techniques. If the conductance value that models the loss of passive components (such as G_d or G_{11}^p and G_{22}^p) is larger than the maximum allowed conductance in step 6, it means that the oscillation is not possible. In this case, we need to go back to step 5 and increase the size of the transistors and repeat steps 6 and 7. But if we are already

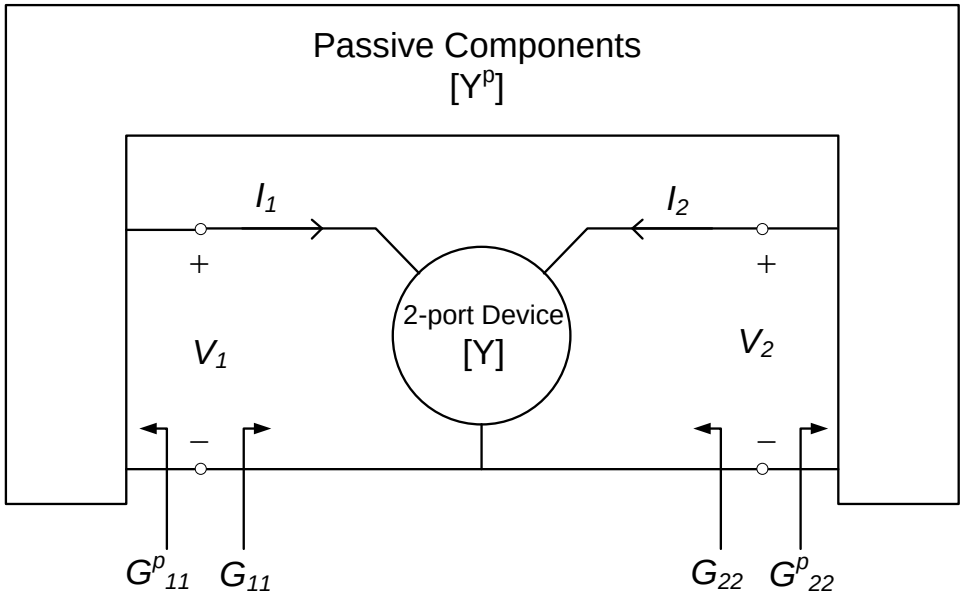


Figure 2.9: Active device embedded in a passive network.

at the maximum size of the transistors based on the restrictions in step 5, then we conclude that the oscillation in the selected f_{osc} is not possible in this process and we need to go back to step 2 to lower f_{osc}. On the other hand, if G_{11}^{p} and G_{22}^{p} satisfy (2.14), then the oscillation is possible. We can simulate the oscillator and verify that the voltage swing is large enough. If not, we need to go back to step 5 or 2 to increase the transistor size or reduce the oscillation frequency. Finally, if the voltage swing is more than is required, we can go back to step 5 and reduce the transistor size to lower the power consumption for the same frequency or go back to step 2 and increase the oscillation frequency.

The flowchart of the above methodology is illustrated in Figure 2.10. It is also noteworthy to mention that if there are any phase noise considerations, one can always choose a topology in step 4 or choose a transistor size in step 5 to trade off the oscillation frequency or power consumption with a better phase noise performance.

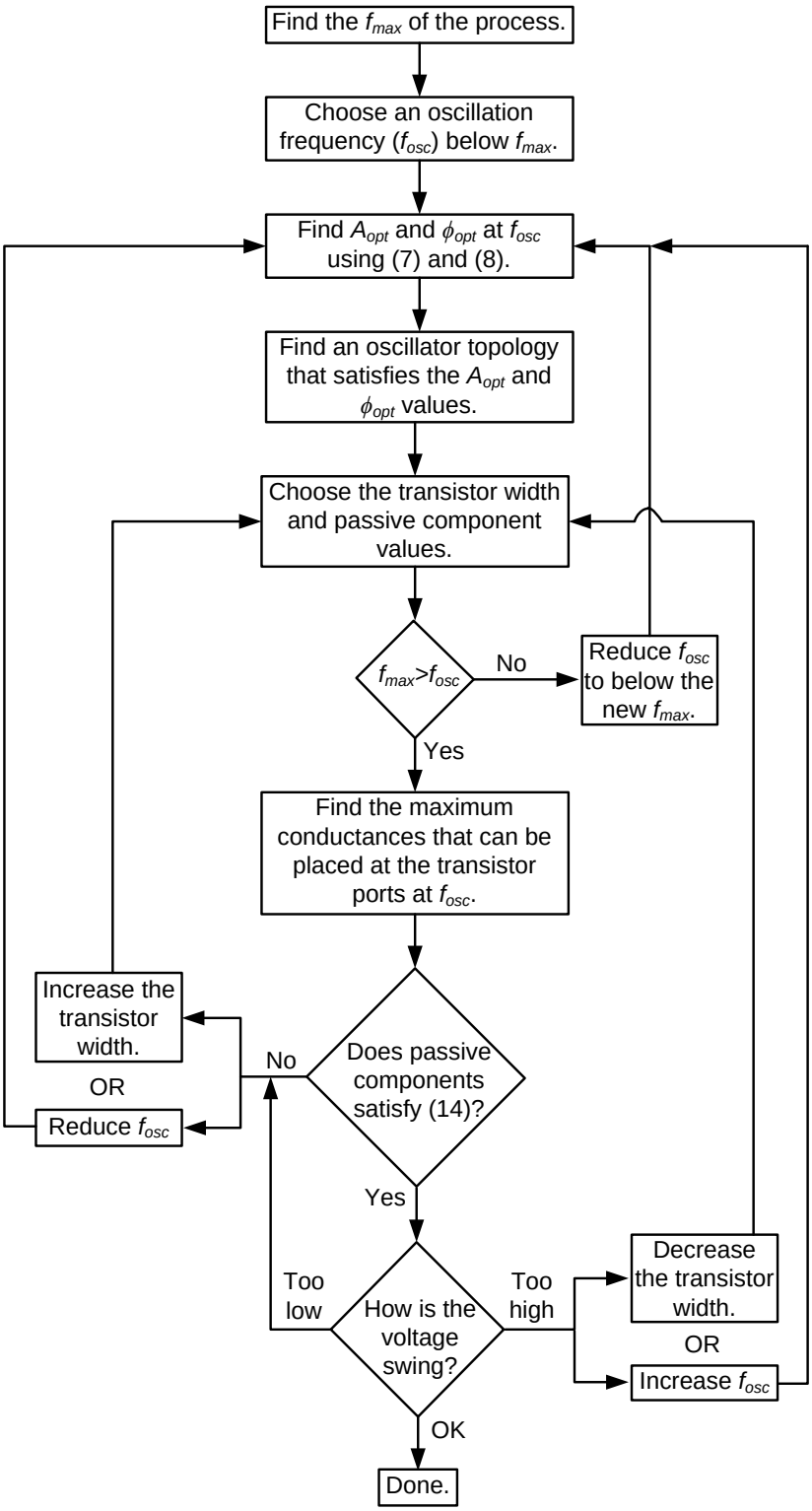


Figure 2.10: Flowchart of the proposed design methodology for high-frequency fundamental oscillators.

2.4 121 GHz and 104 GHz Fundamental Oscillators

2.4.1 Design and Simulation

Using the above methodology we design two fundamental oscillators at 120 GHz and 105 GHz in a 0.13 μm CMOS process. Starting from step 1, we find the f_{max} of the process to be 174 GHz. This number is simulated for a 10 μm wide transistor with 10 fingers and the biasing condition of $V_{ds} = V_{gs} = 1.5$ V. As mentioned before, this f_{max} is based on extrapolation and is more than the typical measured value, which is around 135 GHz [28]. We choose 120 GHz and 105 GHz as oscillation frequencies because they are higher than any reported fundamental oscillation frequency in a 0.13 μm CMOS process and are also lower than the typical f_{max}. For step 3 we plot A_{opt} and ϕ_{opt} as a function of frequency in Figure 2.11. For both frequencies, A_{opt} and ϕ_{opt} are around 1 and 120°, respectively. Therefore, the simplest and closest topology for step 4 is a 3-stage ring oscillator. Next, in step 5 we use the topology of Figure 2.12 to size the transistors and inductors. For initial sizing, the buffer is disconnected from the oscillator. Based on the power budget and reasonable inductor size, we choose $W_1 = 10$ μm with 10 fingers for each transistor, which corresponds to a power consumption of 22 mW for the oscillator. The transistor is implemented using a conventional double gate connection and a substrate contact ring around the transistor as shown in Figure 2.13(a). Using the transistor size, the inductors would be $L_d = 70$ pH and $L_d = 90$ pH for an f_{osc} of 120 GHz and 105 GHz, respectively. In step 6 we need to go back to Figure 2.6 and find G_m which is the maximum G_d that can sustain the oscillation. This figure is plotted for $A = 1$, $\phi = 120°$, and the same transistor size. G_m is 2.4 mS and 2.9 mS for f_{osc} of 120 GHz and 105 GHz, respectively. Having the maximum G_d and the inductor sizes from step 5, we can find the minimum allowed quality factor of the inductors to be 8 and 6

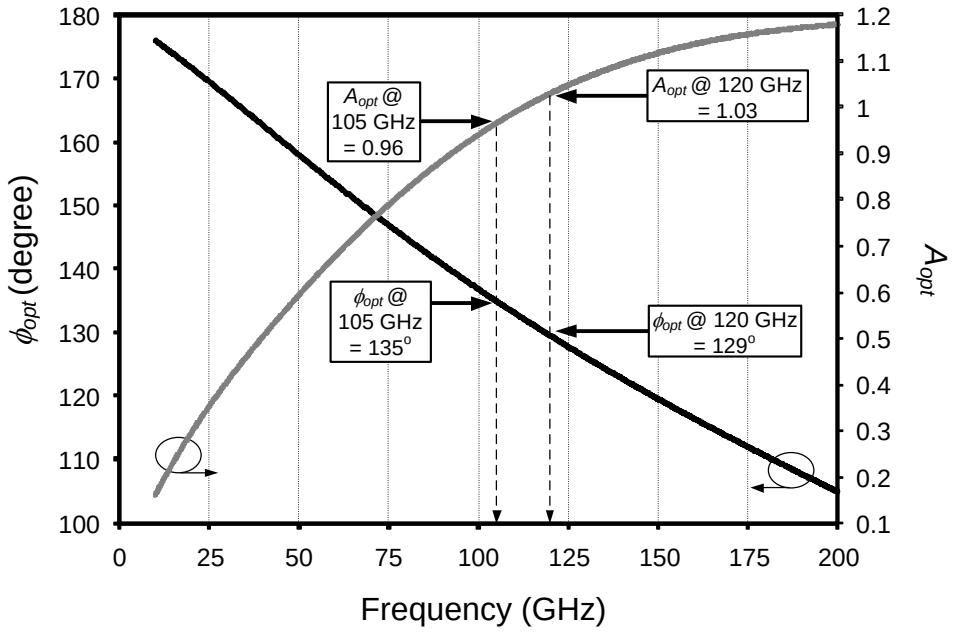


Figure 2.11: Simulation of the optimum A and ϕ for a 0.13 μm CMOS transistor.

for L_d = 70 pH and L_d = 90 pH, respectively. Using Sonnet electromagnetic simulator, we design high quality factor inductors in step 7. To do so, we use shielded coplanar transmission lines as inductors and achieve quality factors of 30 and 26 for L_d = 70 pH and L_d = 90 pH, respectively. These values are higher than the minimum required quality factors (8 and 6) and therefore oscillation is possible. The cross section of the shielded coplanar transmission lines is presented in Figure 2.13(b). In this Figure d_s is the distance between the shield and the signal line and varies between 6 μm to 13 μm for different inductor values.

At this point we can go back to step 2 and increase the oscillation frequency. However, we decide to keep the frequencies at 120 GHz and 105 GHz because as additional loss is added to the circuit from vias and connections, the quality factor of the inductors drops. Furthermore, we require a high voltage swing in order to deliver high output power. As shown in Figure 2.12, a small buffer transistor size of W_2 = 2 μm is used

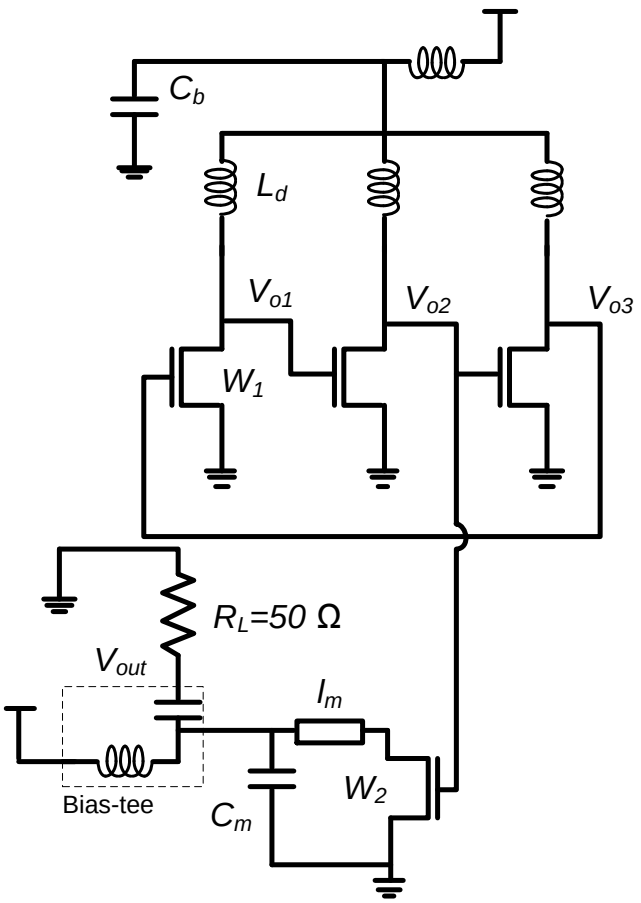


Figure 2.12: A 3-stage ring oscillator with buffer.

to minimize the loading of the oscillator. The buffer consumes 2.7 mW from a 1.5 V supply. To match the buffer to the 50 Ω load, a transmission line similar to that of Figure 2.13(b) with d_s=10 μm and length of l_m along with a capacitor, C_m=62 fF, are used. The matching capacitor, C_m, and the DC supply bypass capacitor, C_b, were constructed using the metal-to-metal capacitors of the probing pads and hence a quality factor of 150 is achieved at 120 GHz. The length of matching transmission lines are l_m=340 μm and l_m=415 μm for the 120 GHz and 105 GHz oscillators and they both have the electrical length of around $\lambda/2$. For these oscillators, the first and second harmonics are out of phase and will be canceled out at the V_{dd} line [29]. However, the 3rd harmonic exists at

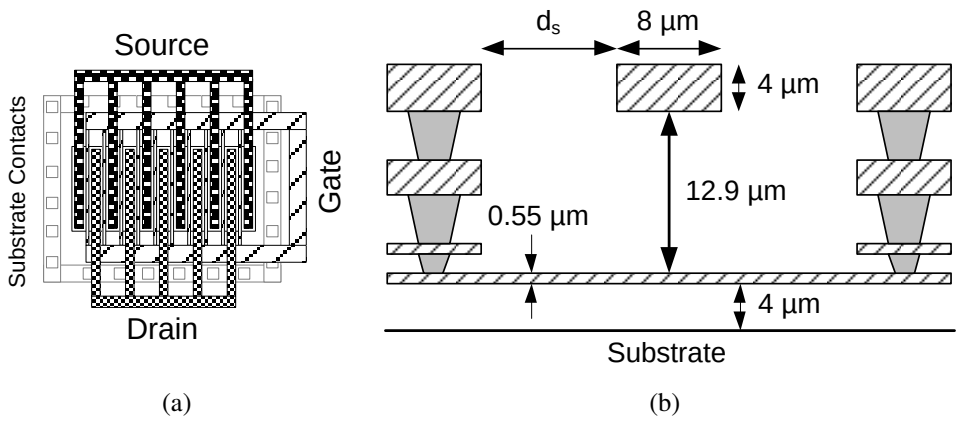


Figure 2.13: (a) Layout of a double-gate connection transistor that is used in all the oscillators and (b) cross section of the shielded coplanar transmission line in the employed 0.13 μm CMOS process.

the V_{dd} line and will be suppressed by C_b.

All of the lines and pads are simulated using Sonnet, and Cadence Spectre was used to find the output frequency and power. After a careful simulation, the output power of -3 dBm and -2 dBm were achieved at 123 GHz and 107 GHz. Figure 2.14 shows the simulation of one period of V_{out}, buffered V_{o2} and unbuffered V_{o2} signals in time domain for the 123 GHz oscillator. Because of the small buffer transistor, the V_{o2} amplitude and frequency do not change very much with the buffer. For the same reason the voltage gain of the buffer is only 0.25. Simulation shows that adding the buffer introduces a maximum phase change of 4° between the output nodes (V_{o1}, V_{o2} and V_{o3}). Phase noise of -85 dBc/Hz and -90 dBc/Hz at 1 MHz offset was simulated for 123 GHz and 107 GHz oscillators, respectively. The power of all other harmonics are at least 45 dB lower than the fundamental signal in both oscillators.

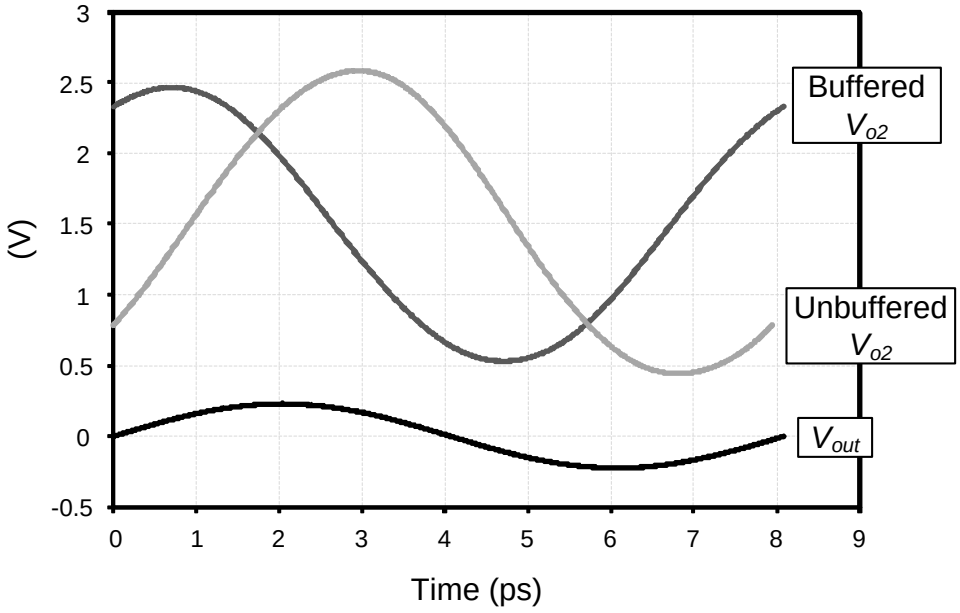


Figure 2.14: Simulation of V_{out}, buffered V_{o2} and unbuffered V_{o2} signals in time domain for the 123 GHz oscillator.

2.4.2 Measurement Results

The fundamental oscillators were fabricated in a 0.13 μm CMOS technology. Figure 2.15 shows the chip photo of these oscillators. A WR-08 GSG Picoprobe with a built-in bias-tee was used to probe the output of these oscillators. Based on the factory data, the insertion loss of the probe is around 2 dB at the measured frequencies. Next, we mix down the signal using an OML WR-08 harmonic mixer and connect the IF port of the mixer to the Agilent 8564EC spectrum analyzer. The oscillation frequency was found by sweeping the LO frequency and measuring the IF frequency change [21]. The measured oscillation frequency for the two oscillators are 121 GHz and 104 GHz, which are in good agreement with the simulation results. Based on the factory data sheet, the typical conversion loss of the harmonic mixer is 47.2 dB and 45 dB at 121 GHz and 104 GHz, respectively. Figures 2.16 and 2.17 show the measured output spectrum of the two oscillators. Based on the loss of the measurement setup, the peak output powers are -3.5

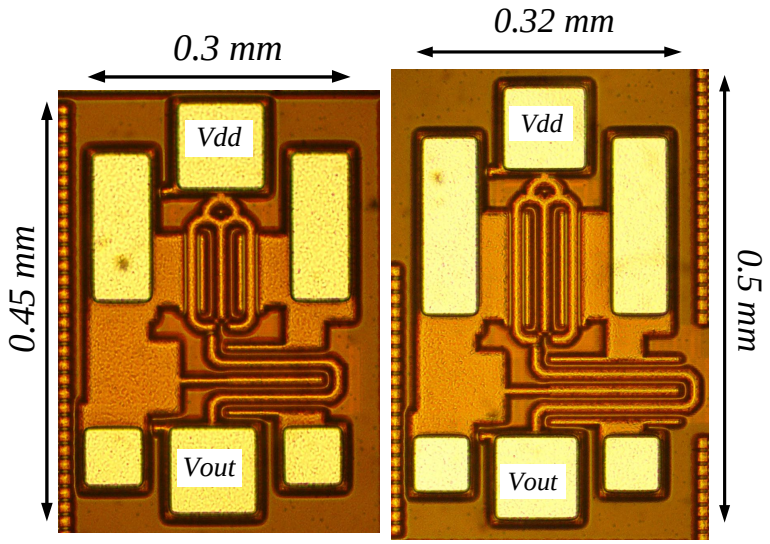


Figure 2.15: Die photo of the fundamental oscillators at (a) 121 GHz and (b) 104 GHz.

dBm and -2.7 dBm at 121 GHz and 104 GHz, respectively. The measured results are close to the simulation presented in the previous section. The DC power consumption including the output buffer is 21 mW from a 1.28 V supply and 28 mW from a 1.48 V supply for 121 GHz and 104 GHz oscillators, respectively. The phase noise at 1 MHz offset frequency was measured to be -88 dBc/Hz and -93.3 dBc/Hz for the 121 GHz and 104 GHz oscillators, respectively. Table 2.1 shows a comparison of this work with the state of the art. To the best of the authors' knowledge, the 121 GHz and the 104 GHz oscillators have the highest output power in any CMOS oscillator and the 121 GHz oscillator has the highest frequency among 0.13 μm CMOS fundamental oscillators.

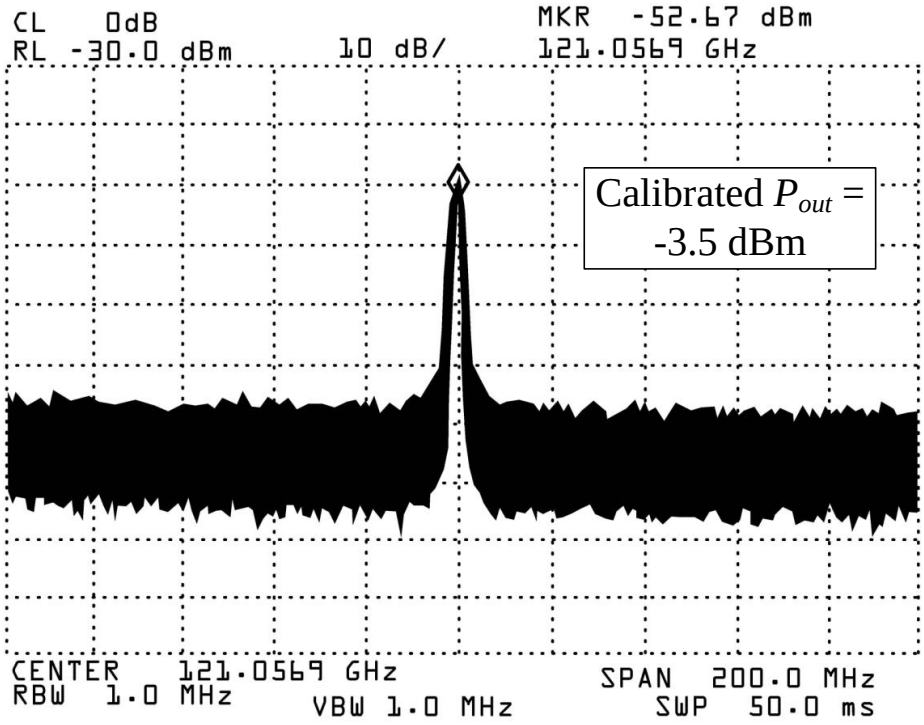


Figure 2.16: The measured IF spectrum of the 121 GHz oscillator.

2.5 256 GHz and 482 GHz Triple-Push Oscillators

For many terahertz applications the target frequency is larger than the maximum oscillation frequency and hence it is desirable to make oscillators beyond the f_{max} of transistors. One example is using conventional CMOS process in the terahertz band. To do so, we need to use higher order harmonic oscillators rather than fundamental oscillators. Push-push oscillator is the most common topology for oscillation beyond f_{max} [20,25]. It collects the second harmonic of the fundamental component and is usually implemented using a cross-coupled oscillator. Recently CMOS harmonic oscillators including push-push structures have been reported at around 300 GHz and beyond [17,19,20]. However the reported output power is less than -45 dBm which is low for most practical applications. Low output power of CMOS terahertz oscillators is one of the major reasons

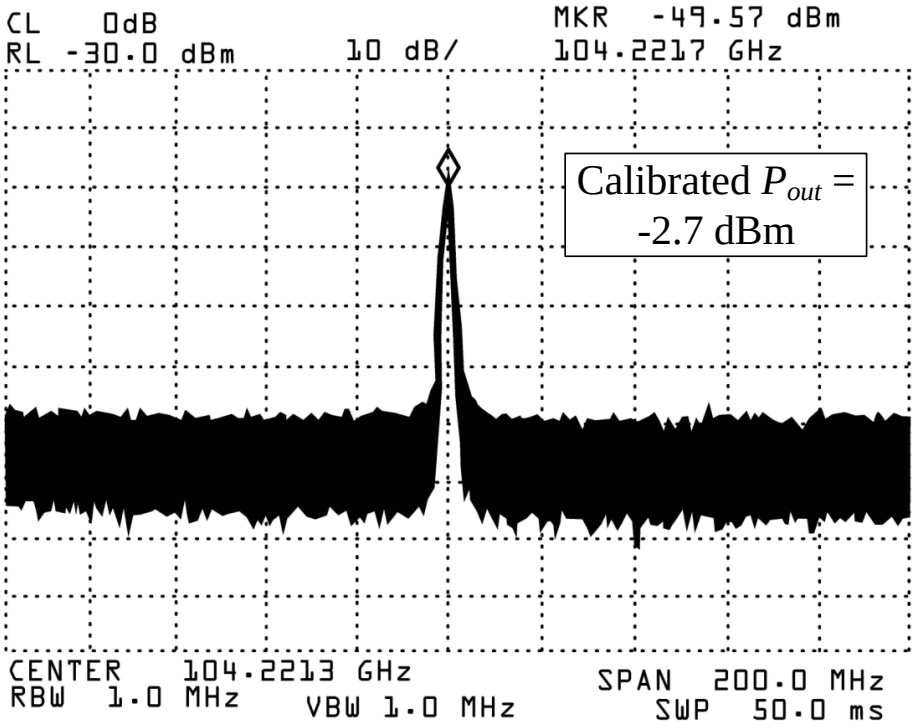


Figure 2.17: The measured IF spectrum of the 104 GHz oscillator.

of why CMOS has not been used to implement a complete terahertz transceiver. In this section, we use two major techniques to boost the power and achieve -17 dBm at 256 GHz and -7.9 dBm at 482 GHz in CMOS: 1- We use the theory introduced above to generate higher power and voltage swing at fundamental frequency and 2- Efficiently transfer the power of the 3rd harmonic from the transistors to the load.

2.5.1 A Triple-Push Oscillator in 0.13 μm CMOS

As discussed in Section 2.3, in the employed 0.13 μm CMOS process, a 3-stage ring oscillator can reach a higher oscillation frequency and at the same time provide a higher voltage swing compared to a cross-coupled oscillator. Higher voltage swings at the

transistor ports increase its nonlinearity. Therefore, a harmonic oscillator that is based on a 3-stage ring structure leads to higher frequency and power than the push-push oscillator. Furthermore, since the 3-stage ring oscillator has one more transistor than the push-push oscillator, it can potentially generate even more output power. The other advantage of the 3-stage ring over a push-push structure is that because the phase shift per section is 120°, the same fundamental frequency requires larger inductors, making them easier to characterize and implement. The proposed topology is shown in Figure 2.18. In this circuit, the phase shift per section is 120° and therefore the third harmonic

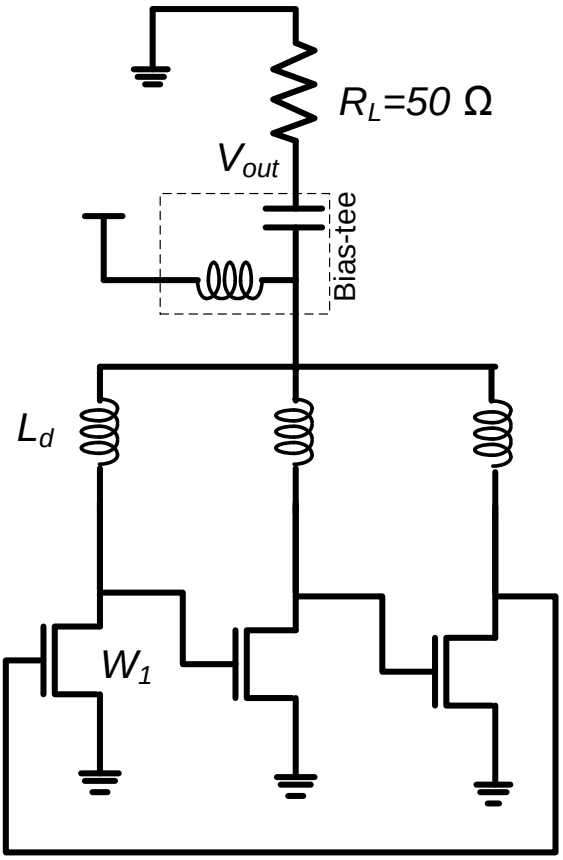


Figure 2.18: A triple-push oscillator based on a three stage ring.

of the fundamental frequency from all three transistors is in phase and hence it adds up constructively at the output node, V_{out}. For the same reason, all the harmonics that are

not multiples of 3 (e.g., 1st, 2nd, 4th and etc) are out of phase and cancel out at node V_{out}. This kind of harmonic oscillator that adds up the third harmonic of the fundamental oscillation at the output is called triple-push [29, 30].

Although the topology in Figure 2.18 can achieve high frequencies in fundamental oscillation, it is not optimized for high power harmonic generation. To increase the voltage swing and hence generate a stronger third harmonic, we propose the topology of Figure 2.19. Let us assume a fundamental oscillation frequency of 85 GHz which

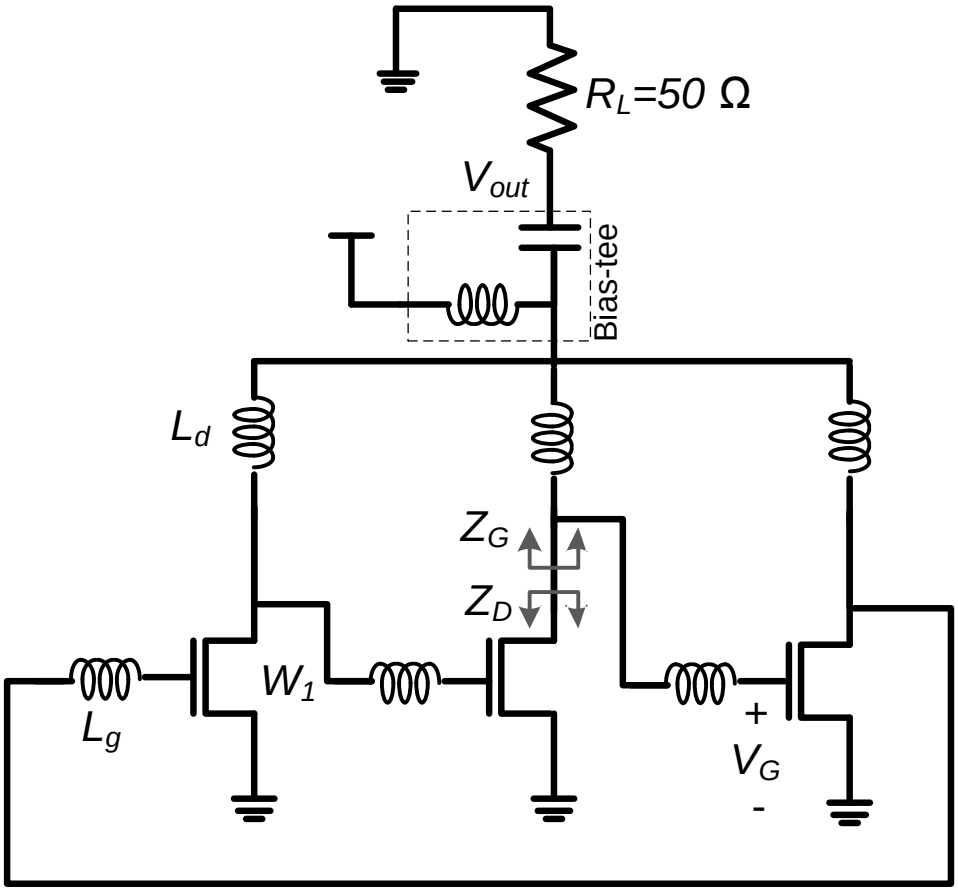


Figure 2.19: Enhanced triple-push oscillator for high power generation.

results in the output frequency of 255 GHz. From Figure 2.11 we know that the optimum conditions for a stand-alone transistor at 85 GHz are A_{opt}=0.84 and ϕ_{opt}=144°. However,

in a regular 3-stage ring in Figure 2.18 A=1 and ϕ=120°. By using an inductor in the gate of the transistor as in Figure 2.19 we can get closer to the optimum values: The inductor delays the voltage and can change ϕ from 120° to the optimum value of 144°. The inductor also resonates with the input capacitance of the transistor and increases the gate voltage to reduce A (i.e., voltage gain of a stand-alone transistor) from 1 to the optimum value of 0.84.

To find the optimum L_g we redraw a transistor and its gate inductor in Figure 2.20. Because the 2-port network in Figure 2.20 is a section of the oscillator shown in Figure

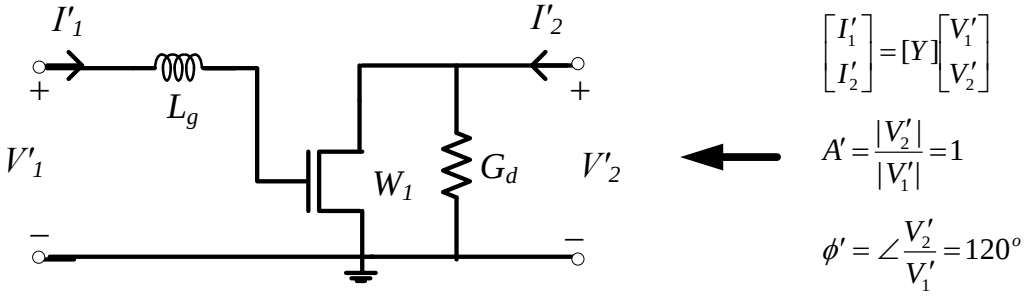


Figure 2.20: The model of one section of the enhanced triple-push oscillator used to optimize the gate inductor value.

2.19, the gain and phase shift of this stage are $A' = 1$ and $\phi' = 120°$. Therefore the activity condition of the network in Figure 2.20 can be found from (2.6) to be

$$G_m = \frac{P'_R}{|V'_1||V'_2|} = -(G'_{11} + G'_{22}) - |Y'_{12} + Y'^*_{21}| \cos(\angle(Y'_{12} + Y'^*_{21}) + 120°) > 0, \qquad (2.15)$$

where Y'_{ij}'s are the elements of the admittance matrix of the network, $G'_{ij} = Real[Y'_{ij}]$, and $i, j = 1, 2$. As it was discussed in Section 2.3.1, G_m is not a direct function of L_d and that is why it is not included in Figure 2.20. G_m in (2.15) is plotted in Figure 2.21 for different gate inductor values and G_d=0. To take into account the effect of inductor loss, we construct L_g using a shielded coplanar transmission line with d_s=5 μm and a resulting quality factor of around 30 at 85 GHz. In this plot, the width of the transistor is W_1 = 20

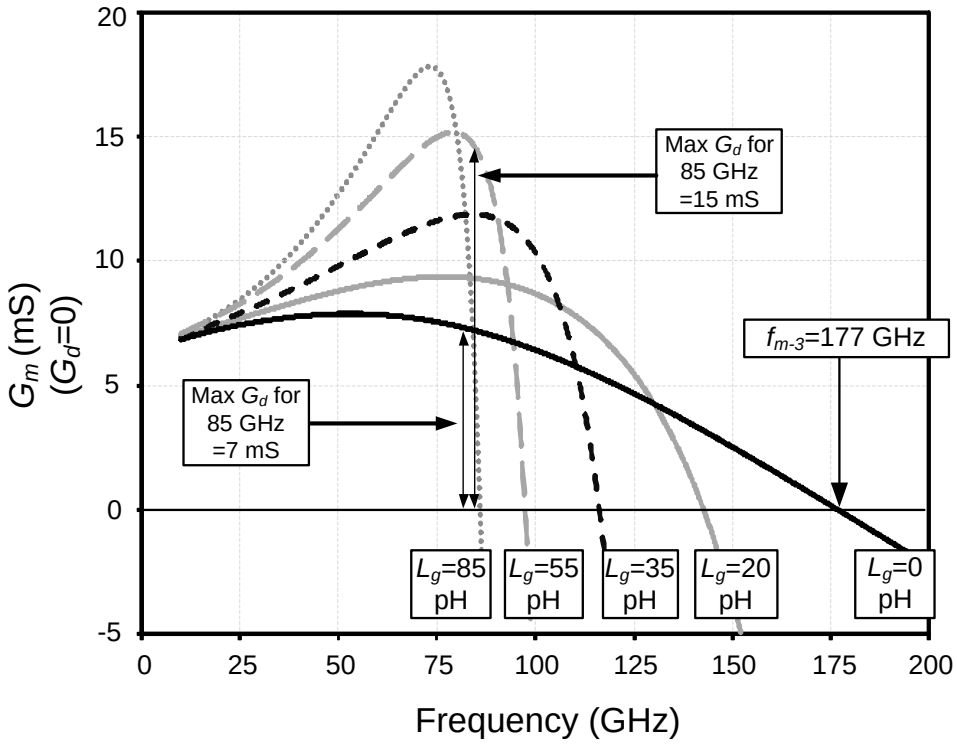


Figure 2.21: Simulation of G_m of one section of the enhanced triple-push oscillator shown in Figure 2.20 with different L_g values using the 0.13 μm CMOS process.

μm with 20 fingers. Figure 2.21 shows that at lower frequencies, the G_m increases with L_g. For example, at 85 GHz, G_m goes from 7 mS to 15 mS as L_g goes from zero to 55 pH. This also implies that for a fixed loss, i.e., fixed G_d, and fixed $|V_1'|$ and $|V_2'|$ at 85 GHz, the transistor shown in Figure 2.20 generates more power for a higher L_g. This higher power generates higher gate voltage swing that results in stronger harmonic generation. For a fair comparison, it should be mentioned that for $L_g = 0$ and $L_g = 55$ pH, the required L_d to keep the oscillation frequency at 85 GHz is $L_d = 68$ pH and $L_d = 45$ pH, respectively. Thus, for a fixed oscillation frequency, as L_g increases, L_d decreases and its corresponding loss, i.e., G_d, increases if the quality factor of different L_d's is the same. In our example, for $L_d = 68$ pH and $L_d = 45$ pH fortunately the increase in $G_d = L_d\omega/Q$ (68 pH/45 pH $\simeq$ 1.5) is less than the increase in G_m (15 mS/7mS $\simeq$ 2.1 from Figure 2.21)

and hence the voltage swing is higher with L_g = 55 pH compared to L_g = 0. Optimum L_g of 55 pH results in maximum G_m in Figure 2.20. Similarly, maximum gate voltage swing in the oscillator in Figure 2.19 happens for around the same L_g value. The gate voltage amplitude at 85 GHz changes from 1.1 V with no L_g to 1.8 V with L_g=55 pH in Figure 2.19. Note that a gate inductor that tunes out the gate capacitor at 85 GHz and results in the highest voltage swing at the gate in the open loop structure is around 120 pH. However, based on Figure 2.21, L_g of greater than 85 pH results in a very low or even negative G_m at 85 GHz and therefore the transistor can not support the high voltage swing for L_g=120 pH. This means that for each frequency there is a minimum L_g value that results in a negative G_m and makes the oscillation impossible as shown in Figure 2.21. In the actual design, the gate inductor should be adequately smaller than this value. To summarize, as shown in Figure 2.21, there is a trade-off between the maximum frequency of oscillation and the power at lower frequency as we change the value of L_g.

The gate inductor L_g also helps extract the harmonic power from the transistor. As shown in Figure 2.19, Z_D is the impedance looking into the drain of the transistor and Z_G is the impedance looking from the drain of the transistor. If Z_D and Z_G are matched at the 3rd harmonic then the transistor delivers the maximum power at this frequency. Assuming that the loss at the gate of the transistor is much lower than the loss at the load, R_L, then after matching Z_D and Z_G, most of the power from the device flows to the load. Figure 2.22 shows the reflection coefficient at the drain of the transistor with and without an optimum L_g for matching the 3rd harmonic. Here, the definition of the reflection coefficient for complex impedances is used [38]. Using an optimum L_g of 20 pH we can achieve the minimum drain reflection coefficient of -9 dB at 255 GHz while the fundamental oscillation frequency is kept at 85 GHz. Without using any L_g the reflection coefficient is -2.2 dB at 255 GHz.

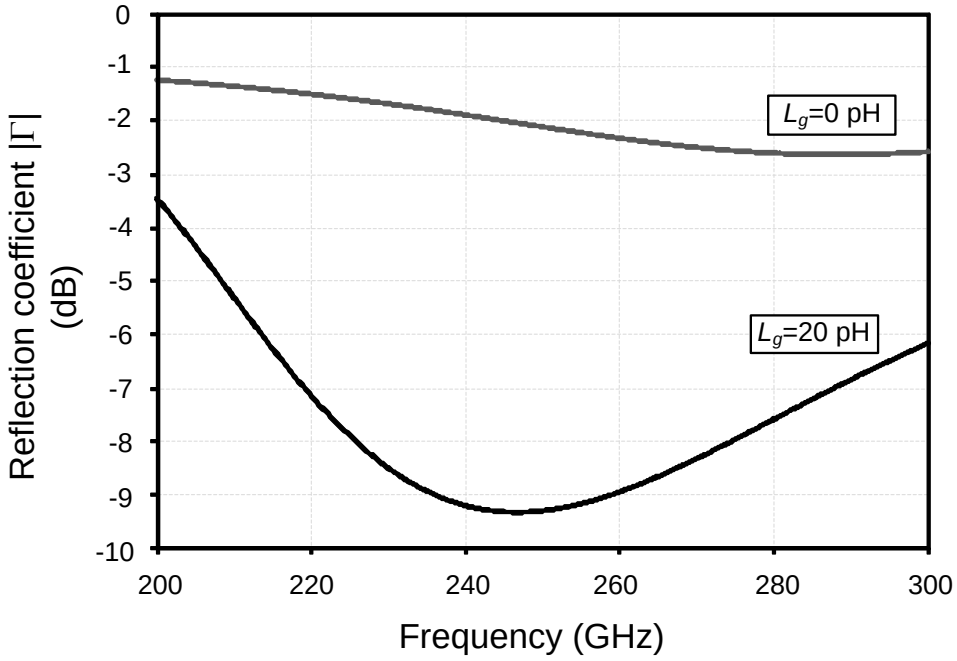


Figure 2.22: Simulated reflection coefficient at the drain of the transistor with and without the gate inductor, L_g.

In the designed prototype we select $W_1 = 20$ μm to increase the third harmonic power and have a reasonable inductor size. L_g and L_d are constructed using shielded coplanar and microstrip transmission lines, respectively. As discussed, L_g can improve both harmonic generation and matching at the same time. However the optimum L_g values for harmonic generation and matching are different. Initial simulation shows that with the optimum component values of $L_g = 30$ pH and $L_d = 50$ pH, the circuit generates maximum power of -3 dBm at 255 GHz. Figure 2.23 shows the gate voltage (V_G) and output voltage (V_{out}) in time domain for L_g=0 and the optimum case of L_g=30 pH. By using this value of L_g, the output power increases by 6 dB.

In order to maintain the symmetry of the layout, we had to deviate from the optimum inductor values. All of the lines, connections, and pads were simulated in the Sonnet electromagnetic simulator. The final simulation shows that the oscillator frequency has

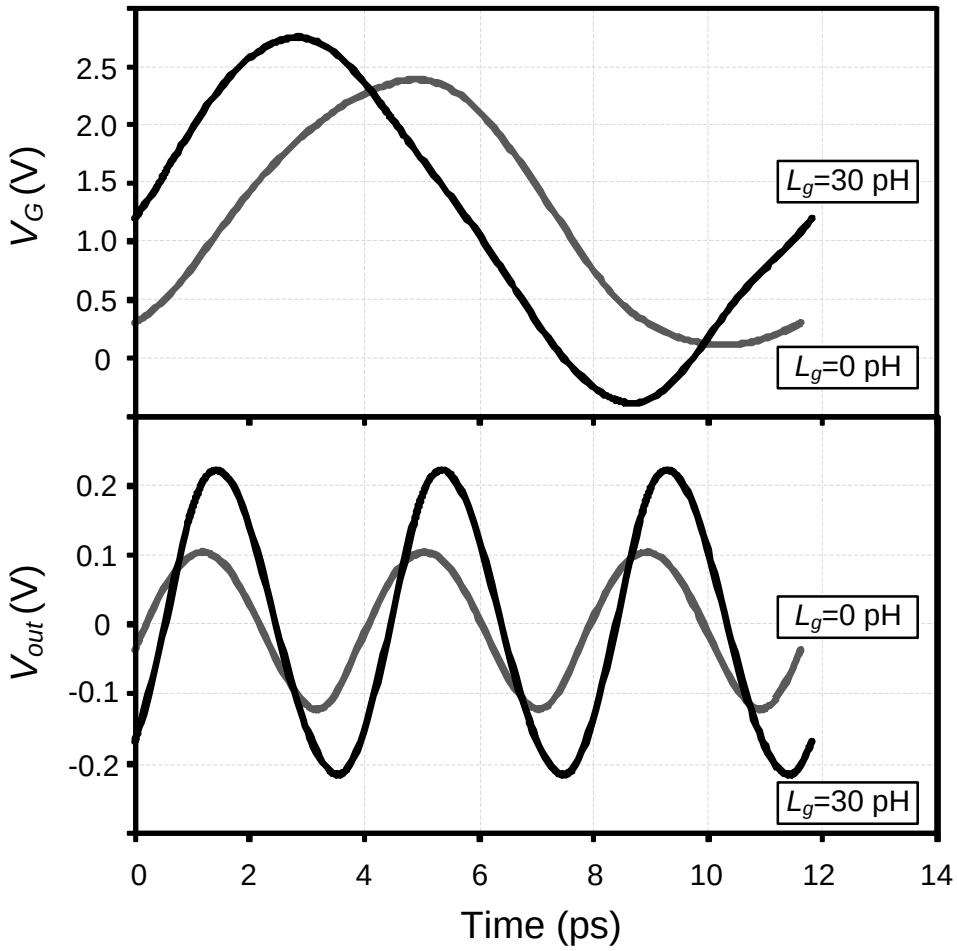


Figure 2.23: Simulated gate voltage (V_G) and output voltage (V_{out}) in time domain for L_g=0 and the optimum case of L_g=30 pH.

a small shift to 260 GHz with -6.4 dBm of power with a DC power consumption of 36 mW from a 1.2 V power supply. The phase noise is simulated to be -83 dBc/Hz at 1 MHz offset. The output spectrum is shown in Figure 2.24. All of the harmonics are at least 20 dB below the 260 GHz component. Figure 2.24 is based on the actual layout simulation that includes all of the non-symmetric effects of parasitics and lines.

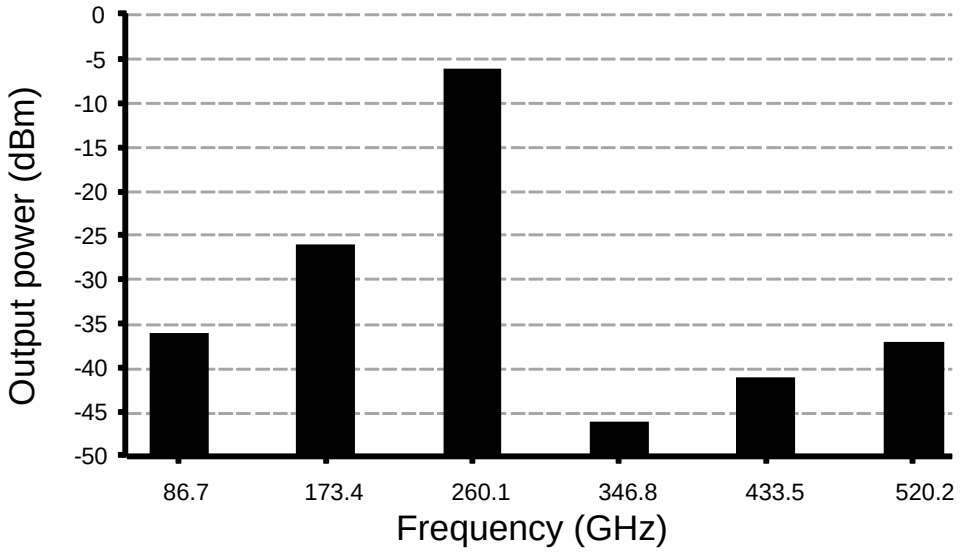


Figure 2.24: Simulated output spectrum for the 260 GHz oscillator in the 0.13 μm CMOS process.

2.5.2 A Triple-Push Oscillator in 65 nm CMOS

Using the same approach, we design and simulate a triple-push 450 GHz oscillator in a 65 nm CMOS process. The fundamental frequency is around 150 GHz. Figure 2.25 shows the simulated optimum A and ϕ (A_{opt} and ϕ_{opt}) as a function of frequency for a transistor with bias current of 12.5 mA and width of W=20 μm with 20 fingers in a 65 nm CMOS process. The transistor is implemented using a conventional double gate connection and a substrate contact ring around the transistor similar to Figure 2.13(a). The optimum values at 150 GHz are A_{opt}=0.56 and ϕ_{opt}=163°. As discussed in the previous section, by adding an inductor in the gate of the transistor we can get closer to these optimum values. The activity condition of a 2-port network similar to that of Figure 2.20 is plotted in Figure 2.26. G_m is plotted for different L_g values which are realized using microstrip transmission lines with a signal metal thickness of 1.3 μm and distance between the signal metal layer and the ground layer of 5.9 μm. The quality

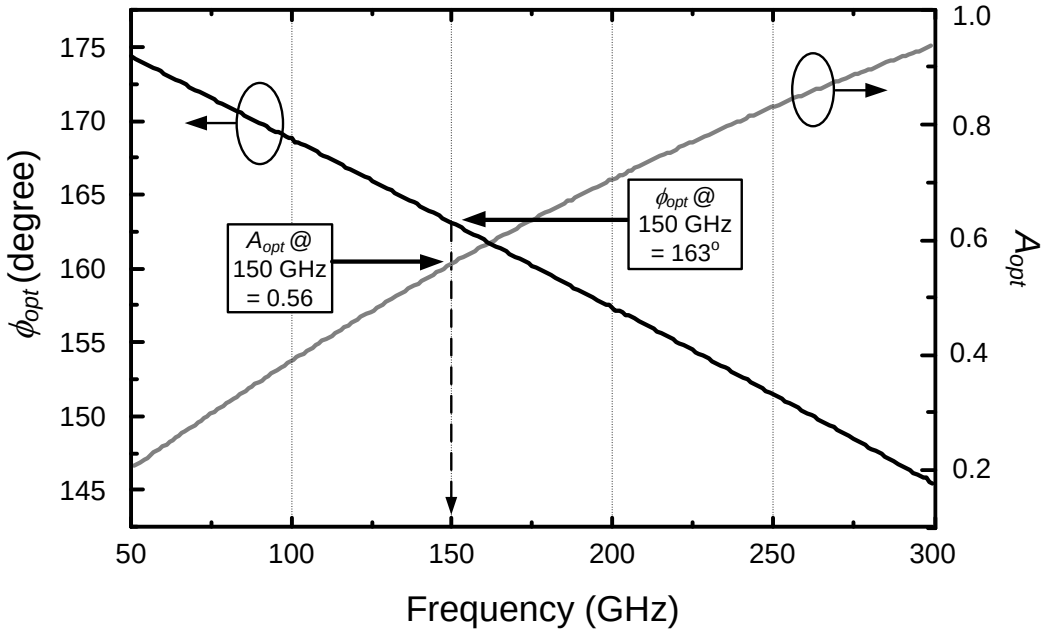


Figure 2.25: Simulation of the optimum A and ϕ of a stand-alone transistor in a 65 nm CMOS process.

factor of the inductors are around 20 at 150 GHz. It is shown in Figure 2.26 that the G_m changes from 9 mS to the maximum value of 33 mS at 150 GHz by adding a gate inductor of L_g=32 pH. As discussed, this gate inductance also results in a maximum voltage swing at the gate of the transistors.

For optimum matching at the 3rd harmonic, the L_g should be around 13 pH. This value results in drain reflection coefficient of -18 dB at 450 GHz. Without L_g, the reflection coefficient increases to -1 dB at 450 GHz. In both cases the output frequency is kept constant at 450 GHz by changing the drain inductor, L_d, which is realized by using the same microstrip transmission line as L_g. The final design employs transistor size of 20 μm and inductor values of Lg=17 pH and Ld=26 pH to reach an optimum voltage swing and power matching for maximum output power. Simulation shows -3 dBm of power at 450 GHz while consuming 38 mW of DC power from a 1.2 V supply. The simulated

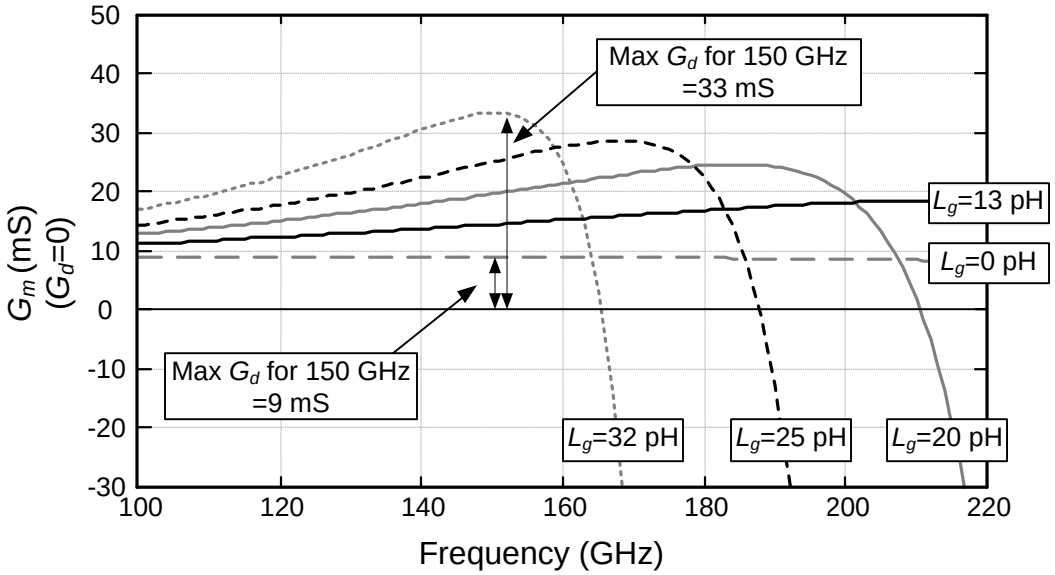


Figure 2.26: Simulation of G_m of one section of the enhanced triple-push oscillator shown in Figure 2.20 with different L_g values using the 65 nm CMOS process.

output spectrum is shown in Figure 2.27. Without using L_g , the simulated power is 18 dB lower at the same frequency.

2.5.3 Measurement Results

Figure 2.28 shows the die photos of the triple-push oscillators. Figure 2.29(a) shows the test setup for the frequency measurement of the 482 GHz oscillator. A Cascade i500-GSG probe with a built in bias-tee is used to probe the output signal as shown in Figure 2.29(a). If we had an on-chip antenna to extract the power from the oscillator we could eliminate the bypass capacitor of the bias-tee since on-chip antennas usually have a series capacitor and block any DC current. Simulation shows that if we use a 50 Ω on-chip antenna, the RF choke of the bias-tee can be replaced by a 150 μm on-chip microstrip transmission line. This adds only around 0.1 dB of loss to the output signal.

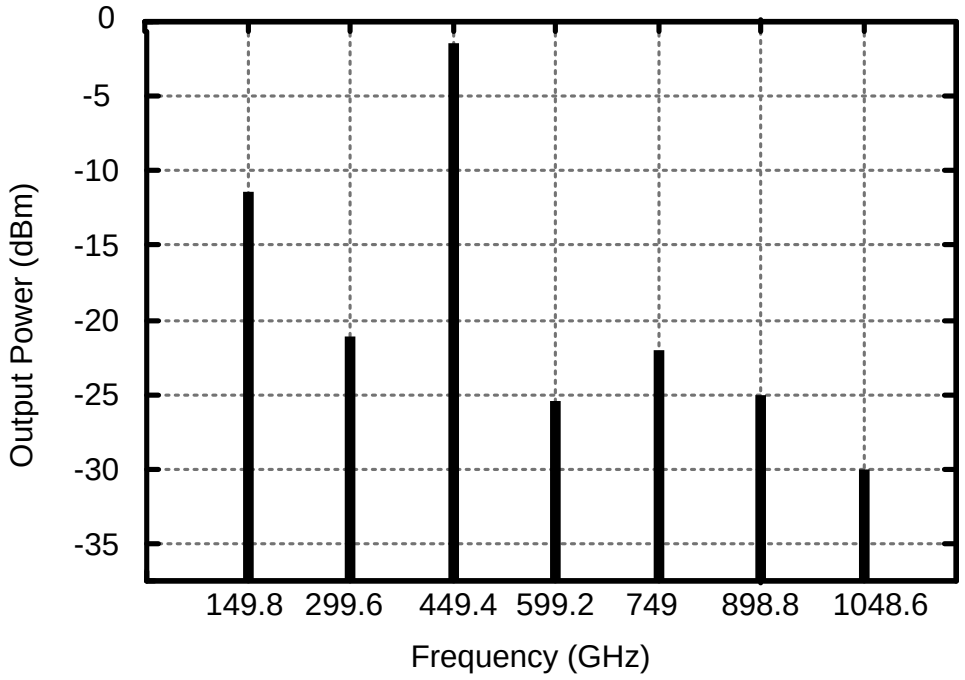


Figure 2.27: Simulated output spectrum of the 450 GHz oscillator in the 65 nm CMOS process.

Therefore we can replace the probe with an on-chip antenna and have a similar performance in both triple-push oscillators. As shown in Figure 2.29(a) a VDI WR-2.2EHM harmonic mixer is connected to the probe to mix down the signal. By sweeping the LO frequency and observing the IF, the LO harmonic number and the signal frequency can be determined. The output frequency was measured to be 482.1 GHz. The difference between simulation and measurement is due to inaccuracy in device models as well as overestimation of the effect of vias. The IF spectrum of the signal is shown in Figure 2.30(a) when the 16th harmonic of the LO frequency is used. In this figure, the power consumption is 35 mW from a 1.2 V supply. The phase noise is measured to be -76 dBc/Hz at 1 MHz offset as shown in Figure 2.30(b). Using the same setup we are able to observe the 2nd harmonic at 321.4 GHz that is very close to the lower cut-off frequency of the WR2.2 waveguide. The loss of the probe and all the other components are

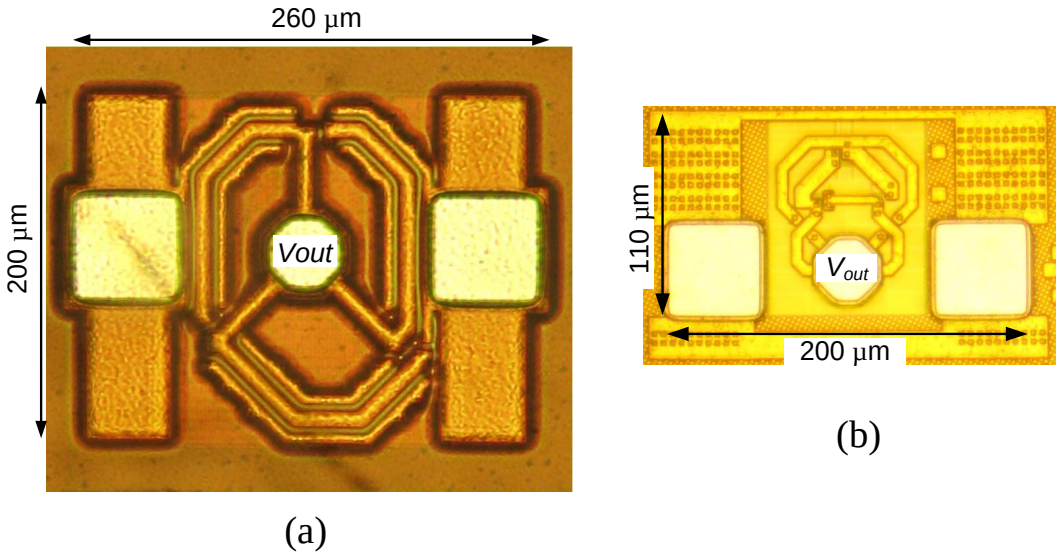


Figure 2.28: Chip photo of the (a) 256 GHz and (b) 482 GHz oscillators.

calibrated using network analyzer by Cascade and VDI. The loss of the probe is 9 dB at 482 GHz and 7 dB at 321 GHz, and the conversion loss of the mixer is 44 dB and 35 dB for the 16th harmonic of the LO when the signal is at around 482 GHz and 321 GHz, respectively. Using these values, we found the power of the 3rd harmonic to be 15.5 dB higher than the 2nd harmonic. With the same setup as Figure 2.29(a), we measured the output power at 482 GHz versus DC power shown in Figure 2.31. To be more accurate, we also used an Erickson PM4 power meter as illustrated in Figure 2.29(b). This measured output power is also shown in Figure 2.31. The measured output power with 35 mW DC power consumption from a 1.2 V supply is -8.6 dBm which is 5.6 dB lower than the simulated output power with similar DC power. This is mainly because of the inaccurate device models at this frequency range. When the DC power consumption increases to 61 mW the peak output power of -7.9 dBm at 482 GHz is achieved. To the best of the authors' knowledge, the output power is the highest among CMOS and SiGe sources and is comparable with oscillators using InP HEMT and InP HBT. Table 2.1 shows the comparison of this work with the state of the art.

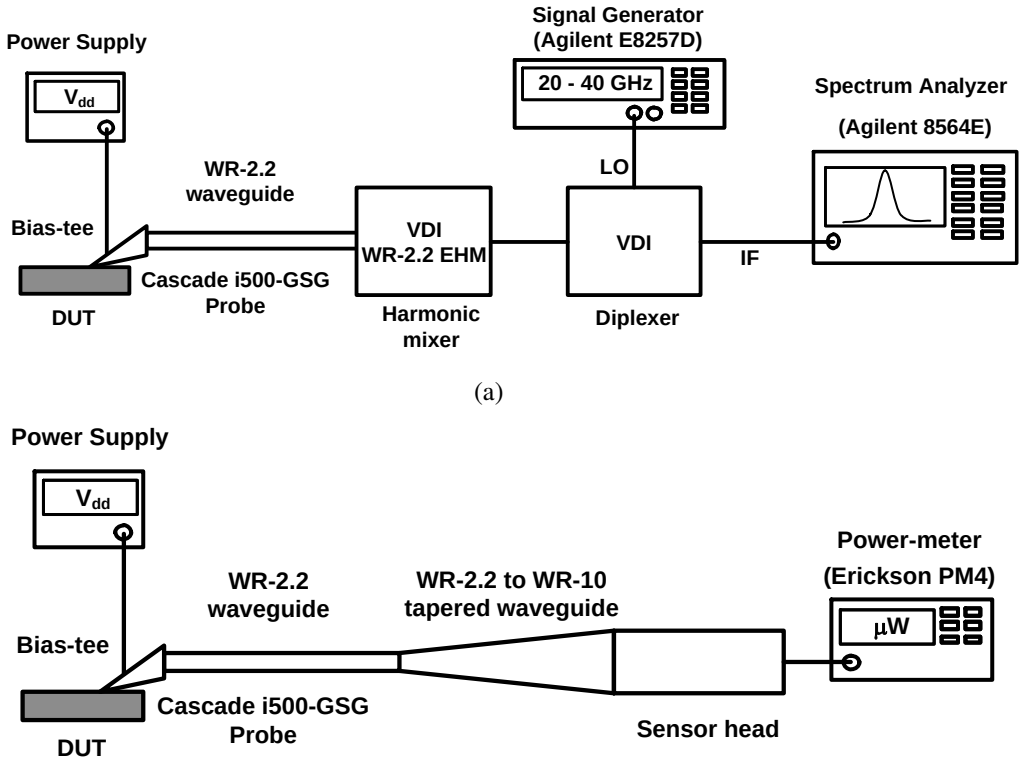
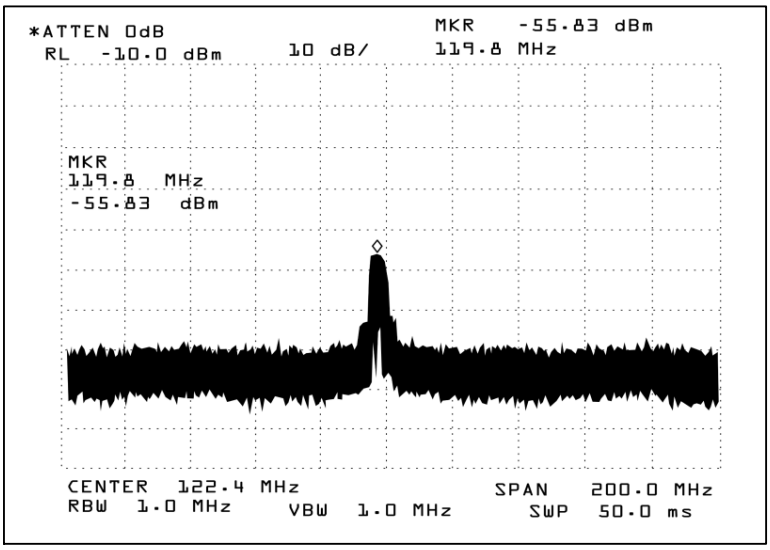
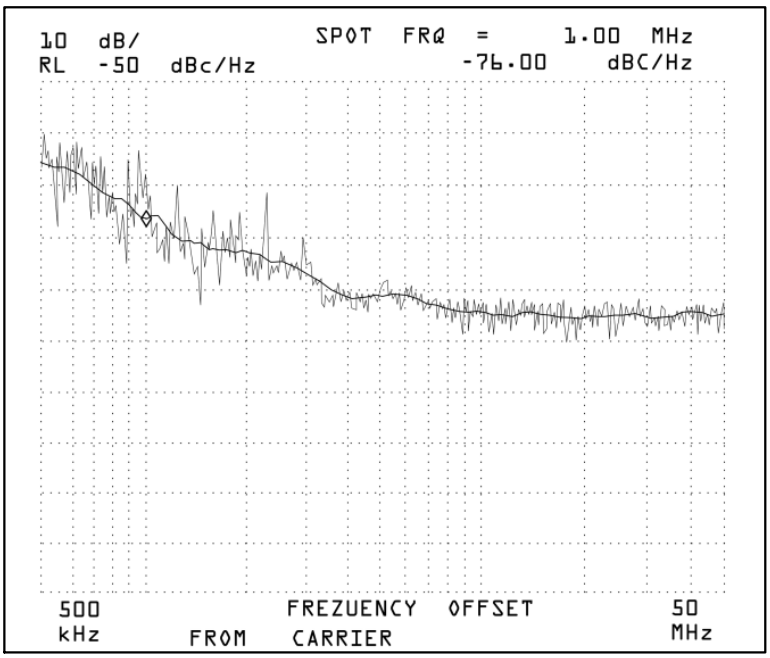


Figure 2.29: Test setup for measuring (a) output frequency and (b) output power of the 482 GHz oscillator.

A similar test setup as in Figure 2.29 was used to measure the output frequency and power of the triple-push oscillator in 0.13 μm CMOS. A Cascade Infinity WR-03 GSG probe with 5 dB loss at around 260 GHz was used to measure the output. The probe has a built-in bias-tee, which was used to bias the circuit from the output node. The signal is mixed down using an OML WR-03 harmonic mixer. To measure the output frequency, we used the same method described for the 482 GHz oscillator. Based on this method, the output frequency is measured to be 256 GHz. Fig 2.32 shows the IF spectrum of this oscillator when the 48th harmonic of the LO frequency is used and the DC power consumption is 38 mW from a 1.25 V supply. Because of the high conversion loss of the harmonic mixer, the power received by the spectrum analyzer is low and hence it is



(a)



(b)

Figure 2.30: (a) The measured IF spectrum of the 482 GHz signal for the 16th harmonic of the LO frequency when the power consumption is 35 mW from a 1.2 V supply and (b) its measured phase noise.

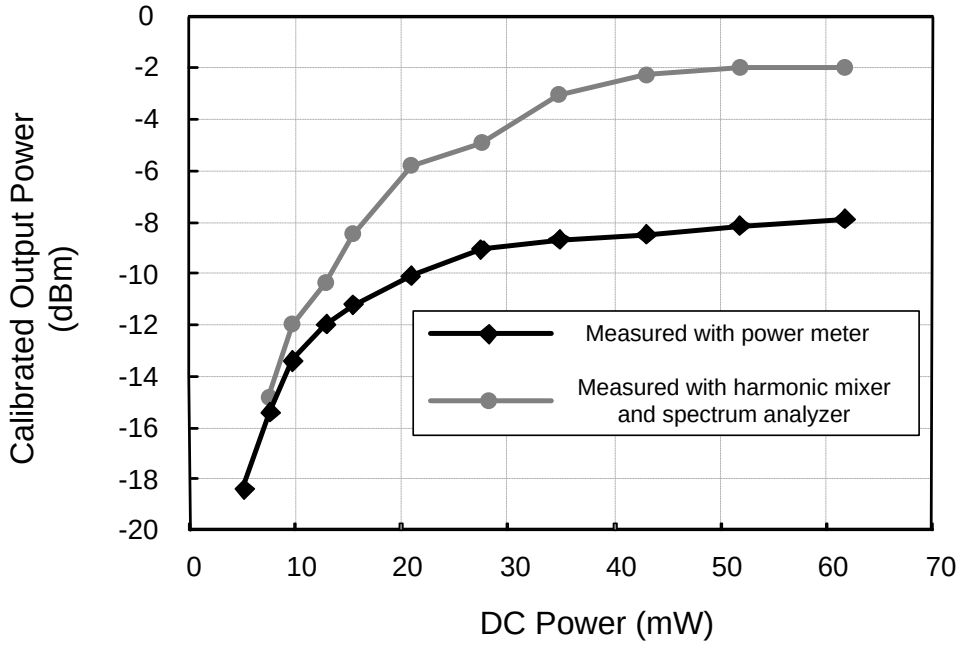


Figure 2.31: The measured output power at 482 GHz as a function of DC power consumption.

hard to measure the phase noise directly from the 256 GHz signal. Similar to [19], to estimate the phase noise, a copy of the same oscillator was implemented with a common source buffer to take out the fundamental frequency. The fundamental signal at around 85 GHz has a high voltage swing and its phase noise can be measured from the buffer to be -97 dBc/Hz at 1 MHz offset. Because the third harmonic is used at the output, the estimated phase noise of the 256 GHz signal would be 9 dB higher than that of the fundamental. Hence the estimated phase noise is around -88 dBc/Hz at 1 MHz offset. To measure the output power we used the same Erickson PM4 power meter as illustrated in Figure 2.29(b). Output power of -19 dBm and -17 dBm was achieved at 256 GHz while consuming 38 mW and 71 mW of DC power, respectively. These values are around 12.6 dB lower than the simulated values. The main reason is that since the oscillator operates above the f_{max} of the transistors, the device models are not accurate. Table 2.1 compares this work with the state of the art. To the best of the authors' knowledge, this oscillator

has the highest power reported in any CMOS or SiGe process in this frequency range and has the highest frequency reported in a 0.13 μm CMOS process.

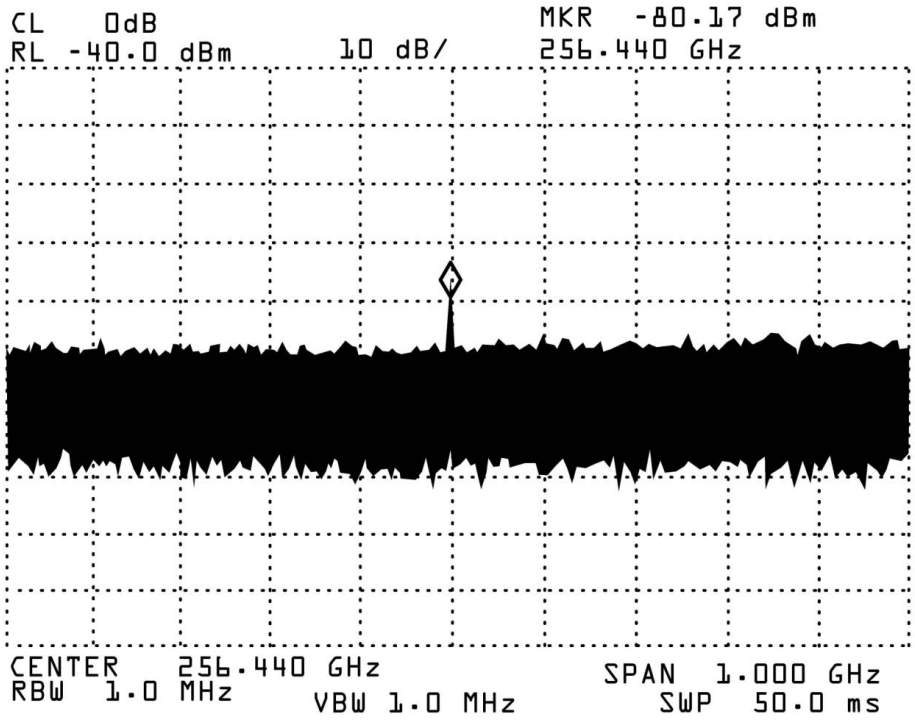


Figure 2.32: The measured IF spectrum of the 256 GHz signal for the 48th harmonic of the LO frequency when the power consumption is 38 mW from a 1.25 V supply

2.6 Conclusion

We have introduced a systematic method to design high power oscillators that can achieve frequencies close to the f_{max} of the transistors. We have also demonstrated a novel triple-push structure to realize CMOS oscillators in the terahertz band. This approach has applications in millimeter-wave frequencies for communication and radar systems as well as terahertz band for bio- and molecular spectroscopy and imaging.

Table 2.1: Comparison with prior art

Ref.	Type	Technology	Frequency (GHz)	Power (dBm)	Phase Noise (dBc/Hz)	DC Power (mW)
[21]	Fundamental	90 nm CMOS	128	-37	-105 @ 10 MHz	9
[22]	Fundamental	90 nm CMOS	104	-8	NA	6.5
[24]	Fundamental	SiGe (f_{max}=300 GHz)	106	+2.7	-96.6 @ 1 MHz	337
[13]	Fundamental	InP (f_{max}=600 GHz)	254	-8	NA	11.7
[12]	Fundamental	InP (f_{max}=650 GHz)	346	-11	NA	115
[15]	Fundamental	InP (f_{max}=600 GHz)	330	-5.7	NA	15.8
[19]	Superposition	90 nm CMOS	324	-46	-91 @ 10 MHz (est.)	12
[20]	Push-push	45 nm CMOS	410	-47	NA	16.5
[36]	Push-push	0.13 μm CMOS	192	-20	-100 @ 10 MHz (est.)	16.5
[25]	Push-push	SiGe (f_{max}=275 GHz)	190	-4.5	-73 @ 1 MHz	215
[39]	Push-push	SiGe (f_{max}=275 GHz)	278	-25	NA	132
This work	Fundamental	0.13 μm CMOS	104	-2.7	-93.3 @ 1 MHz -105 @ 10 MHz	28
This work	Fundamental	0.13 μm CMOS	121	-3.5	-88 @ 1 MHz -102 @ 10 MHz	21
This work	Triple-push	0.13 μm CMOS	256	-17	-88 @ 1 MHz (est.)	71
This work	Triple-push	65 nm CMOS	482	-7.9	-76 @ 1 MHz	61
This work	Triple-push	65 nm CMOS	482	-9	-76 @ 1 MHz	27.5

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CHAPTER 3

A HIGH GAIN 107 GHz AMPLIFIER IN 130 nm CMOS

3.1 Introduction

Millimeter-wave and terahertz frequencies are increasingly used for various applications. Broadband wireless access (e.g., WiMax), vehicular radar, short-range communication, and imaging are among growing applications of mm-wave frequencies [1, 2]. Other applications such as detection of concealed weapons, cancer diagnosis, semiconductor wafer/device inspection, along with bio/molecular spectroscopy for explosive and illegal drug detection, food quality control, and breath analysis for disease diagnosis are being developed and investigated in terahertz frequencies [3, 4].

Implementation of these systems on CMOS is attractive as it offers low-cost and reliable fabrication of various analog and digital blocks on the same chip. However, signal amplification using CMOS transistors is challenging at these frequencies. This is because the operation frequency is close to the maximum oscillation frequency (f_{max}) of the transistors and therefore the maximum available gain (G_{ma}) of the transistors drops below useful level for most applications. In order to boost G_{ma}, neutralization and unilateralization is widely used [5–7]. The maximum theoretical gain of a unilateral device is equal to Mason's invariant function, U. However, fundamentally the maximum achievable gain (G_{max}) of the transistor is higher than U.

In this paper, we introduce a methodology to boost G_{ma} to the G_{max} of the device which is approximately 4 times larger than U. This method creates the optimal termination conditions for the maximum gain. To show the feasibility of the proposed approach, we designed and implemented a 107 GHz amplifier in a standard 130 nm CMOS pro-

cess with typical measured f_{max} of 130 GHz. The amplifier has a gain of 12.5 dB, PAE of 4.4%, and saturated output power of >2.3 dBm consuming 31 mW from a 0.95 V supply. To the best of our knowledge, this work has the highest center frequency in 130 nm and 90 nm processes and its performance is comparable with amplifiers in 65 nm CMOS process in the same frequency range.

3.2 Maximizing the power gain of a transistor

Maximum available gain, G_{ma}, of a transistor is a well known quantity and is defined as the power gain of a two-port device when the ports are simultaneously conjugate matched to the source and load. At frequencies close to f_{max} of the device, G_{ma} is low and matching device ports does not result in sufficient gain. In order to get useful gain at these frequencies neutralization is widely used to cancel the effect of gate-drain capacitor (C_{gd}) of CMOS transistors. This is also called unilateralization because it increases the reverse isolation and hence creates a unilateral device.

It can be shown that if a two port device is unilateralized with lossless passive components, the maximum power gain of the resulting unilateral device is equal to Mason's invariant function, U, which is also known as unilateral gain [8]. In other words, if the C_{gd} of a transistor is canceled, its G_{ma} is increased to the new value of U. For a 3-terminal device as a linear 2-port network shown in Figure 3.1, U is

$$U = \frac{|Y_{21} - Y_{12}|^2}{4(G_{11}G_{22} - G_{12}G_{21})}, \tag{3.1}$$

in which Y_{ij}'s are the elements of the admittance matrix of the network, $G_{ij} = Real[Y_{ij}]$, and $i, j = 1, 2$. The intriguing property of U is that it is invariant under any 4-port, linear, lossless, reciprocal embedding shown in Figure 3.2. This means that for any 2-port device such as a transistor, U is only a function of the inherent characteristics of the

device and not the embedding components.

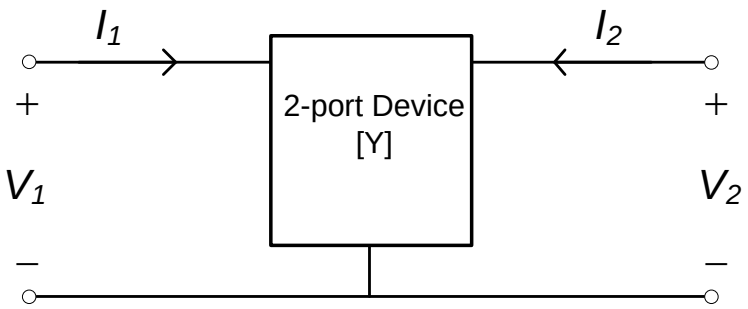

Figure 3.1: A 3-terminal 2-port device.

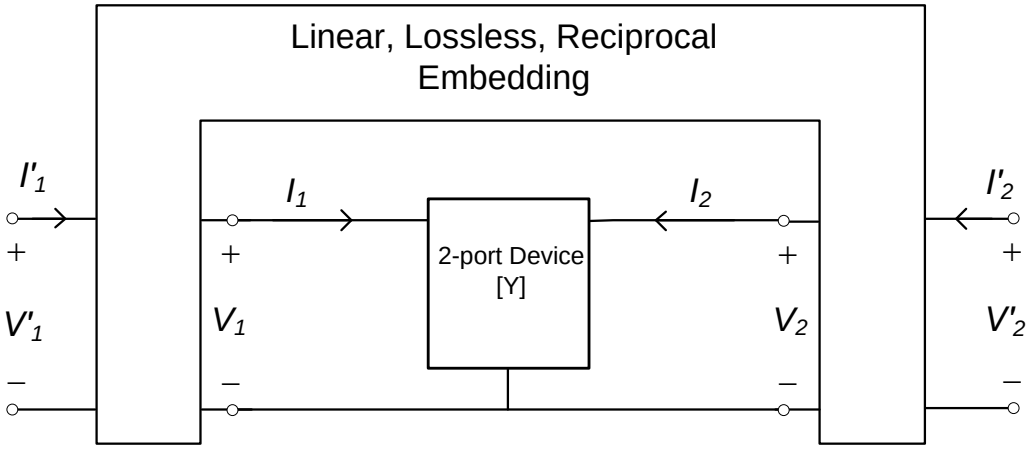

Figure 3.2: A device embedded in a 4-port, linear, lossless, reciprocal network.

Although unilateralization results in higher power gain, its maximum theoretical gain value, U, is lower than the maximum power gain that can be achieved by the device. Assuming that the maximum stable gain (G_{ms}) of the device is much larger than 1, it can be shown that the maximum achievable power gain of the device embedded in a linear, lossless and reciprocal network is

$$G_{max} = (2U - 1) + 2\sqrt{U(U-1)} \simeq 4U, \tag{3.2}$$

in which G_{max} is equal to $4U$ if U is much larger than 1. In other words, if a device is embedded in an optimal lossless passive network similar to Figure 3.2 and then the resulting embedded device is conjugate matched to the load and source, the power gain is around 6 dB higher than the unilateral device. Figure 3.3 shows G_{ma}/G_{ms}, U and G_{max} of a 40 μm transistor in a 130 nm CMOS process.

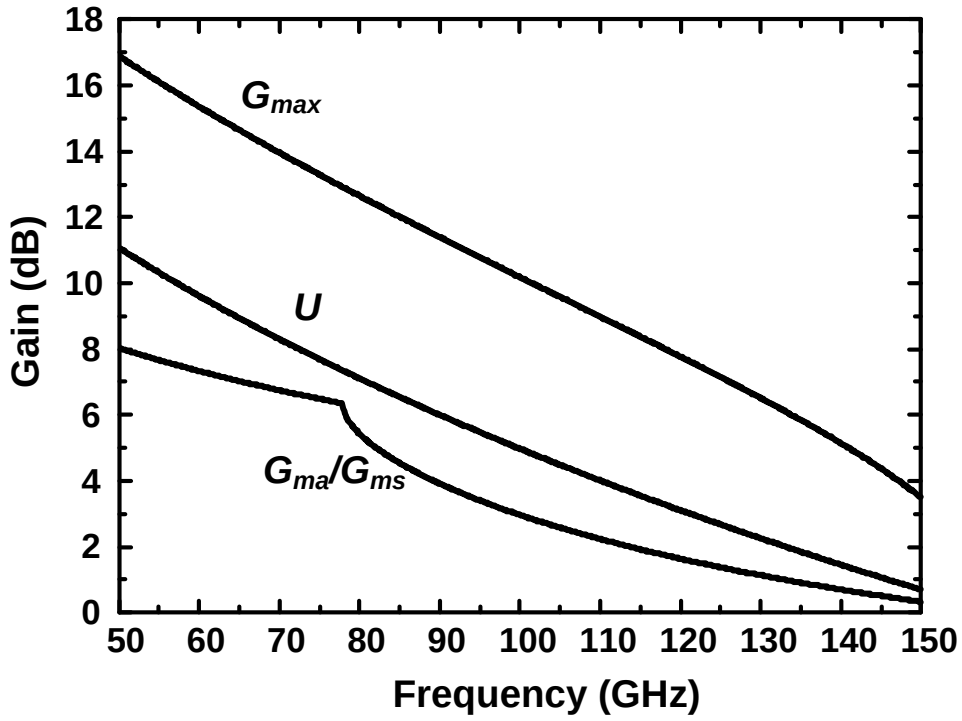

Figure 3.3: Simulated unilateral gain (U), maximum available and stable gain (G_{ma}/G_{ms}) and maximum achievable gain (G_{max}) of a 40 μm transistor in a 130 nm CMOS process.

In order to find the optimum embedding to reach G_{max} we first find the real power flowing out of the device, P_R. For the device in Figure 3.1, we can write this power as

$$P_R = -Re\{V_1^* I_1 + V_2^* I_2\}, \tag{3.3}$$

in which "*" denotes the complex conjugate. Using the definition of the admittance

matrix, P_R can be expressed as

$$\frac{P_R}{|V_1|^2} = -(G_{11} + A^2 G_{22}) - A|Y_{12} + Y_{21}^*| \cos(\angle(Y_{12} + Y_{21}^*) + \phi), \tag{3.4}$$

in which

$$A = \frac{|V_2|}{|V_1|}, \quad \phi = \angle\frac{V_2}{V_1}. \tag{3.5}$$

Assuming most of the source power flows into the transistor and most of P_R flows to the load, the power gain of the device is maximized if the right hand side of (3.4) is maximized: For the same $|V_1|$ (i.e., the same input power), maximum P_R (i.e., output power) results in maximum power gain of the device. For a given device, Y parameters are constant and therefore (3.4) is maximized by

$$A = A_{opt} = \frac{|Y_{12} + Y_{21}^*|}{2G_{22}} \tag{3.6}$$

and

$$\phi = \phi_{opt} = (2k + 1)\pi - \angle(Y_{12} + Y_{21}^*), \tag{3.7}$$

in which k is an arbitrary integer. Figure 3.4 shows the optimum gain and phase conditions for the same 40 μm transistor in a 130 nm CMOS process using (3.6) and (3.7).

At 105 GHz, Figure 3.4 shows that the optimum gain, A_{opt}, is 1.6 and the optimum phase, ϕ_{opt}, is 133°. Simulation of a common source amplifier using the same transistor with simultaneous input and output match using ideal passive components at 105 GHz shows a power gain of 2.5 dB which is exactly equal to the predicted value of G_{ma} in Figure 3.3. In this amplifier A and ϕ are 0.5 and 86°, respectively. These values are far from the optimum values and an appropriate passive embedding should be used for the transistor to improve the conditions and therefore increase the power gain. Different embedding networks can be employed to create the optimum conditions for the transistor. One way to do this is to add an inductor, L_{gd} between gate and drain of the transistor

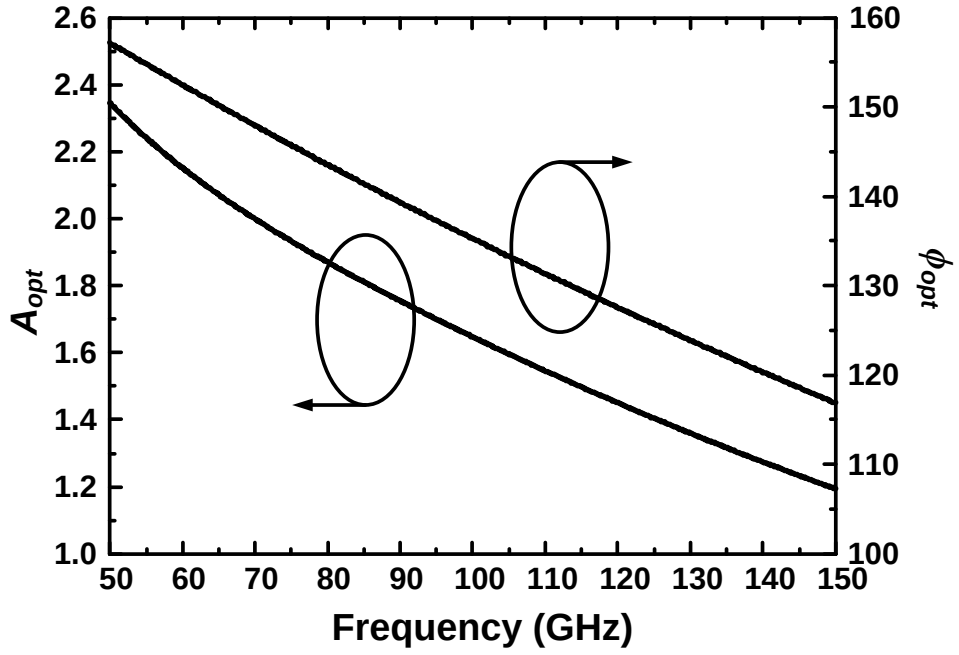

Figure 3.4: Simulated optimum gain (A_{opt}) and phase (ϕ_{opt}) conditions for a 40 μm CMOS transistor in a 130 nm process.

as shown in Figure 3.5. This inductor helps improving both phase and gain conditions. Intuitively, L_{gd} partially resonates with C_{gd} and creates a higher impedance looking into the drain of the transistor and therefore increases the voltage gain of the transistor from 0.5 to the optimum value of 1.6. Moreover, L_{gd} controls the phase shift between input and output of the transistor and therefore can increase ϕ from 86° to the optimum value of 133° at 105 GHz. Figure 3.6 shows simulated G_{ma}/G_{ms} of the transistor in Figure 3.5 for different values of L_{gd}. It can be seen that at peak frequencies, the available power gain is very close to G_{max} which is the maximum achievable power gain of the device. This is made possible by providing the optimum conditions for the transistor at these frequencies.

Figure 3.6 shows that the optimum L_{gd} for the center frequency of 105 GHz is 120 pH. Simulation of a common source amplifier using L_{gd}=120 pH with simultaneous

input and output match at 105 GHz shows a power gain of 7.1 dB and gain and phase conditions of A=2.2 and ϕ=132° which are close to the predicted optimum values. The difference between simulated A and A_{opt} is due to the fact that using only one passive element (L_{gd}), it is almost impossible to simultaneously achieve both optimal gain and phase conditions. In the next section, we use the same technique to design a 107 GHz amplifier with 12 dB of gain in the same 130 nm CMOS process.

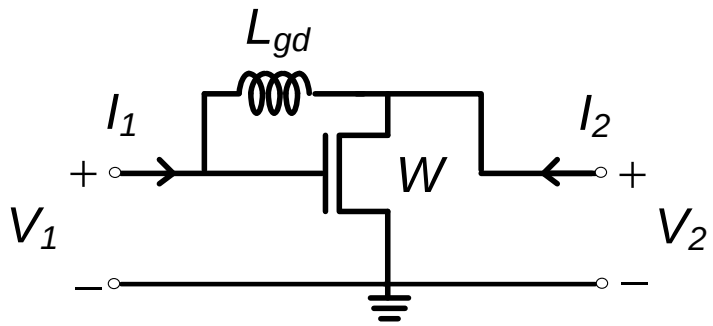

Figure 3.5: A CMOS transistor with a gate-drain inductor (L_{gd}) to improve the available power gain.

3.3 A 107 GHz Power Amplifier

3.3.1 Design Procedure

Figure 3.7 shows the simplified schematic of the proposed amplifier in a 130 nm CMOS process with a typical measured f_{max} of 130 GHz [9]. The amplifier uses three identical stages. The input frequency for this prototype is selected to be around 105 GHz because of the available vector network analyzer which operates up to 110 GHz. All the inductors are implemented using regular or shielded microstrip transmission lines.

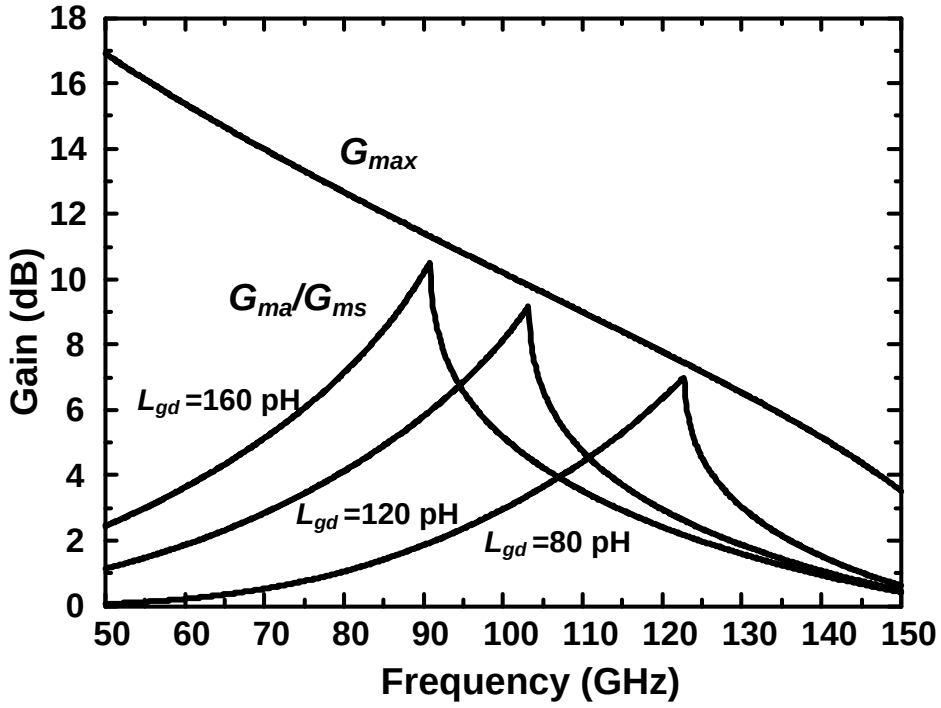

Figure 3.6: Simulated maximum available and stable gain (G_{ma}/G_{ms}) of the transistor in Figure 3.5 for different values of L_{gd}.

The capacitors including the bypass capacitors are implemented using metal finger capacitors or the capacitance of the input and output pads. The Sonnet electromagnetic simulator was used to design all the passive components. C_{m1} and L_{m1} are used to match the input and C_{m2}, L_{m2} and C_{m3} are used to match the output of the amplifier to the 50 Ω source and load impedances, respectively.

Implementing a 120 pH high quality factor gate-drain inductor at 105 GHz is challenging. Because the two nodes of the inductor should be connected to the same device, using transmission line would result in a long inductor with several bends which reduces quality factor of the inductor and creates an odd shape for the inductor layout. The two nodes of spiral inductors can be close to each other but they usually exhibit much lower quality factor than transmission line inductors at these frequencies. To solve this prob-

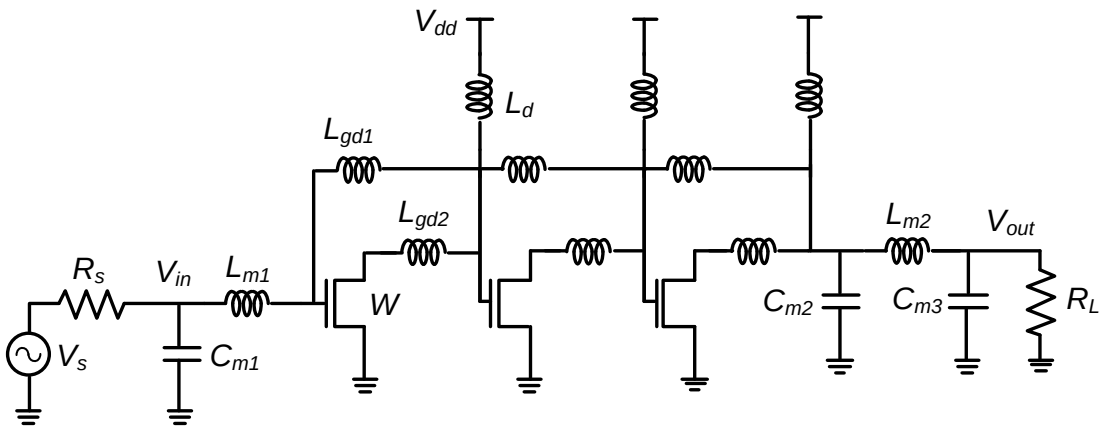

Figure 3.7: Simplified schematic of the proposed amplifier.

lem, L_{gd2} is added to the circuit. This inductor reduces the size of L_{gd1} for the same optimal gain and phase conditions. As a result, all the inductors can be easily implemented using microstrip transmission lines. Furthermore, L_{gd2} is used to connect the stages together, removing the parasitics of lines between the stages. L_{gd2} and L_d are also designed to have a good matching between the stages. Special attention is paid to stability of the amplifier. In designing the amplifier, a few dB of gain is sacrificed to ensure enough margin for unconditional stability at all frequencies. In the final design the components L_{gd1}=55 pH, L_{gd2}=34 pH, L_d=36 pH and a transistor size of W=40 μm with 25 fingers are used. The quality factor of implemented inductors is around 30 at 105 GHz. Simulation shows 15 dB of gain, 10 dB of noise figure and saturated output power of 3 dBm at 105 GHz.

3.3.2 Experimental Results

Figure 3.8 shows the die photo of the implemented amplifier. To reduce substrate coupling the entire structure is shielded by a lower metal layer. Two W-band Cascade

ACP110L probes along with an Agilent 8510XF vector network analyzer were used to measure the amplifier. Figure 3.9 shows the measured small signal S-parameters of the circuit as a function of frequency. Maximum gain of 12.5 dB is achieved at 107 GHz. Reverse isolation is better than 20 dB across the band and at 107 GHz input and output reflection coefficients are -13 dB and -19 dB, respectively. The 3-dB bandwidth of the amplifier is >5.4 GHz. The measured output power, power added efficiency (PAE) and gain is plotted in Fig 3.10 as a function of input power at 107 GHz. Output 1-dB compression point of -1 dBm, maximum output power of 2.3 dBm and maximum PAE of 4.4% are achieved at 107 GHz. This amplifier is unconditionally stable for all the frequencies and power levels. The circuit consumes 31 mW of DC power from a 0.95 V supply.

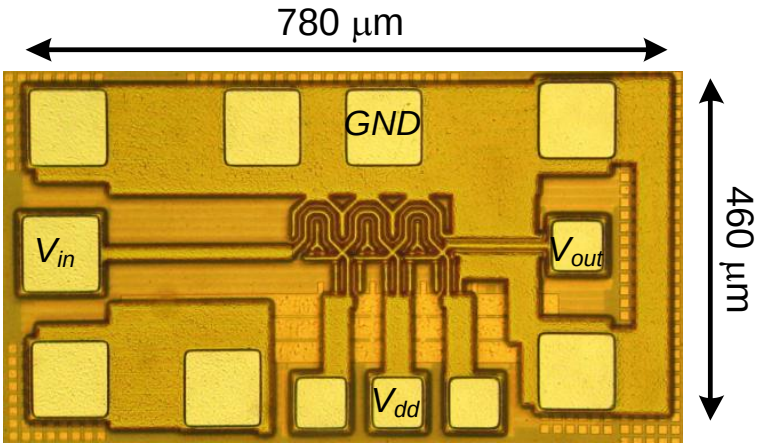

Figure 3.8: Die photo of the 107 GHz amplifier in a 130 nm CMOS.

The comparison with the state of the art is provided in Table 3.1. The center frequency of this amplifier is higher than any other reported amplifier in 130 nm and 90 nm CMOS process. Other specifications such as gain and PAE is comparable to amplifiers in 65 nm CMOS process while consuming 1/3 of the DC power.

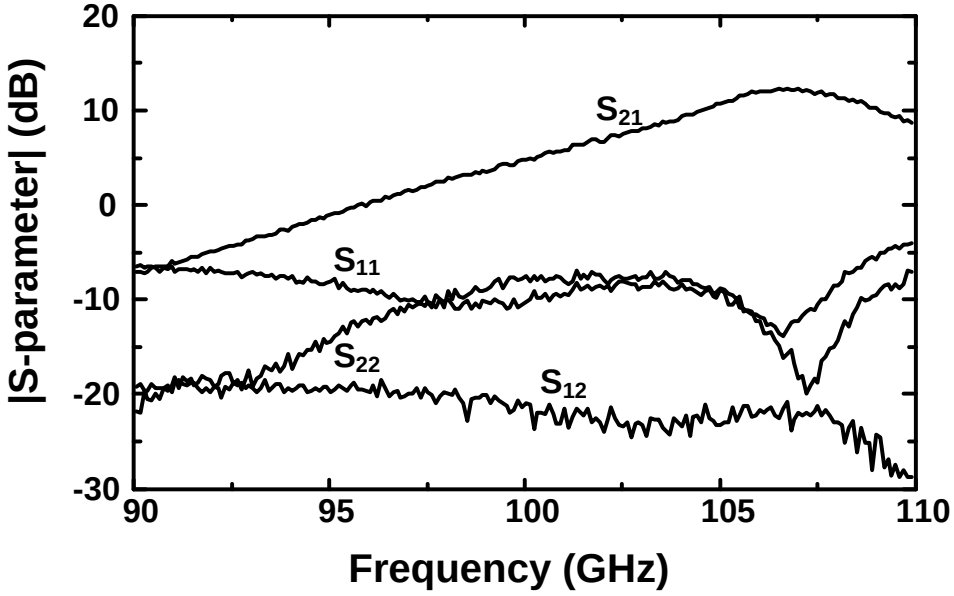

Figure 3.9: Measured small-signal S-parameters as a function of frequency.

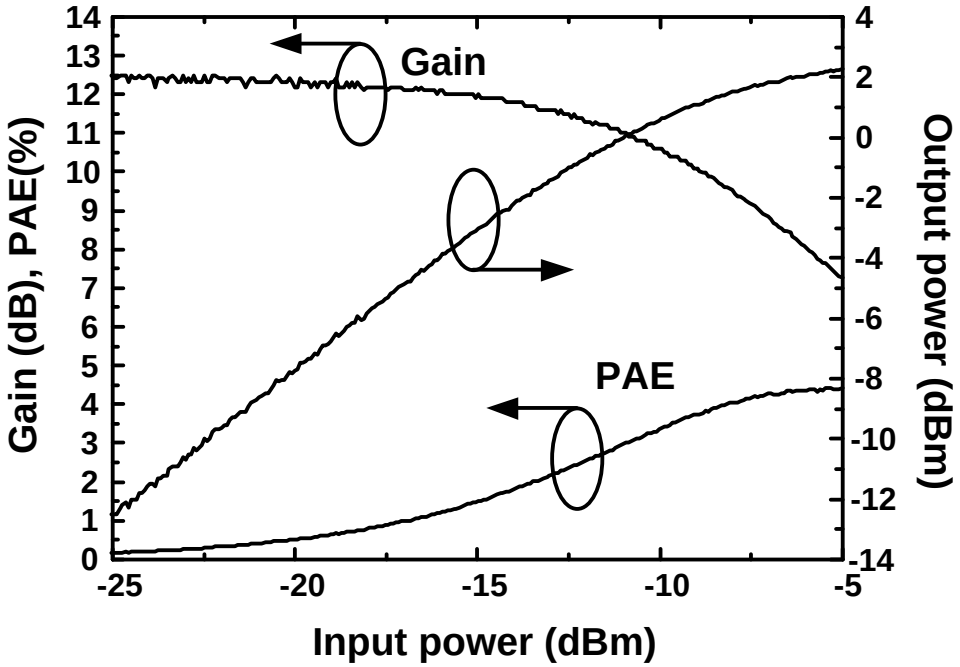

Figure 3.10: Measured output power, PAE and power gain as a function of input power at 107 GHz.

Table 3.1: Comparison with prior art

Ref.	This work	[9]	[10]	[1]	[2]
Technology	130 nm CMOS	130 nm CMOS	90 nm CMOS	90 nm CMOS	65 nm CMOS
Frequency (GHz)	107	60	96	104	94
Gain (dB)	12.5	12	16	9.3	14
NF (dB)	10 (sim)	8.8	NA	NA	7.5
P_{1dB} (dBm)	-1	2	2	NA	6.2
P_{sat} (dBm)	>2.3	NA	4	NA	10
Max PAE (%)	4.4	NA	NA	NA	7.3
V_{dd} (V)	0.95	1.5	2.5	1	1.2
P_{DC} (mW)	31	54	54	22	86

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CHAPTER 4

ELECTRICAL PRISM: A HIGH QUALITY FACTOR FILTER FOR mm-WAVE AND TERAHERTZ FREQUENCIES

4.1 Introduction

The terahertz frequency range is usually defined to be from 100 GHz to 10 THz. Bio- and molecular spectroscopy were the first and the main applications for the terahertz region [1]. Recently, this range also been used for imaging, compact range radars, and remote sensing [2–5]. Traditionally, the solid-state version of all these systems, along with the terahertz sources, have been built using III-V based HBT/HEMT technologies like GaAs [2]. As the CMOS technology scales down, the f_{max} of the transistors are reaching the lower part of the terahertz range, and the 65nm CMOS technology already has an f_{max} of around $200GHz$ [6]. The CMOS scaling along with the III-V technology drawbacks such as cost and efficiency paved the way for the recent terahertz work in silicon processes [7, 8].

The 2-D electrical lattices are two-dimensional discrete lattices in which the building block is constructed using passive elements. Figure 4.1 is an example of a 2-D lattice. Each line represents an inductor, and each dot represents a capacitor to ground. This specific lattice is a low-pass lattice, but other lattices with different frequency responses can be constructed. The 2-D electrical lattices on silicon have a potential in terahertz signal generation and processing due to their distributed nature and their scalability for higher frequencies. Several studies have been done that make this class of circuits promising for high frequencies. In terms of *signal generation*, [9] illustrates the highest output power for a power amplifier for the wide band of $60GHz$ to $90GHz$ using a 2-D electrical lattice. It is also shown in [10] that by using a well-sized nonlinear 2-D lattice one is

able to generate an output signal frequency five to six times greater than the input signal frequency. Because of the distributed nature of this lattice, the power of the input signals will add together to generate the output signal that has more power than each input. In terms of *signal processing*, [11] shows that using low-pass, 2-D lattices it is possible to make an ultra-fast Fourier transformer for terahertz frequencies. Furthermore [12] and [13] demonstrate compact electrical lens in high-pass and anisotropic 2-D electrical lattices, and [14] illustrates 2-D frequency-scanned leaky-wave antenna using the same kind of 2-D lattices. Electrical lattices of this class are known as metamaterials. Interesting phenomena such as negative refractive index is observed in metamaterials at wavelengths much larger than its unit cell dimensions [15, 16].

In all of the terahertz systems, high quality factor filters are the essential part of the operation. Furthermore, the solid-state terahertz sources use nonlinear elements for up/down conversion and multiplication to generate power. To suppress harmonics generated and to get a clean spectrum, a high quality factor filters are required. In terahertz spectroscopy, in order to find the output spectrum, high quality factor filter bank is used. Typically, this is been done off-chip by mixing down the signal and using the filter bank at low frequencies. In order to eliminate the mixer and make a silicon-based spectrometer, a high quality factor filter at terahertz frequencies is desirable. It can be shown that the quality factor of the conventional passive filters are limited to the quality factor of the individual components [17], which is low at high frequencies due to ohmic and substrate loss in silicon processes [18].

In optics, high quality factor filters and demultiplexers have been realized using photonic crystals [19, 20]. By engineering the crystal's frequency band gap, different frequencies will propagate in different directions in the crystal. This spatial filter is called a superprism. The light propagation in this kind of photonic crystal is very sim-

ilar to that in diffraction grating [21]. In other words the dispersion that causes the superprism effect originates from scattering (*e.g.* diffraction grating). In this paper, we introduce a spatial filtering method (electrical prism) using low-pass 2-D electrical lattice. The operation of this filter relies on the dispersion in the 2-D electrical lattices. Unlike superprism, dispersion in the homogeneous 2-D electrical lattice originates from the discreteness of the lattice rather than the scattering [22]. Due to this dispersion, the direction of the energy flow is a function of signal frequency at frequencies close to the cut-off frequency. The main specifications of the proposed filter are as follows:

- The negative effective index is observed in this electrical prism.
- Unlike metamaterials, these interesting features are happening close to the cut-off frequency, which helps to channel the signal from input to output.
- The quality factor of the filter is much larger than the quality factor of each individual component in the lattice, solving one of the major challenges of high frequency filter design mentioned above.
- The operating frequency of this filter can be as high as the cut-off frequency of a 2-D electrical lattice which can reach 1.4 THz in a conventional CMOS process.

The rest of this paper is organized as follows. In Section 4.2, the general theory of plane-wave propagation in a low-pass, 2-D lattice will be discussed. The direction of the energy will be derived for rectangular and triangular lattices. In Section 4.3 we will show how to build an electrical prism using 2-D lattices. Filter quality factor discussion, theory, and simulation plots will be provided for a lossless structure. The effect of component loss on the quality factor of the filter will be discussed in Section 4.4. In Section 4.5, the design, simulation and the measurement result of the electrical prism prototype will be presented. We will then summarize the paper in section 4.6.

4.2 plane-wave Propagation in 2-D Lattices

4.2.1 Rectangular Lattice

Figure 4.1 shows a top view of a 2-D rectangular lattice. The lines represent inductors with value L, and the dots are the nodes that are connected to ground with capacitors with value C. The dot distances are h_1 and h_2 in the $\hat{x}$ and $\hat{y}$ directions respectively. Coordinate vectors for the nodes, $\vec{d_1}$ and $\vec{d_2}$, and the position vector $\vec{r}$ are defined as

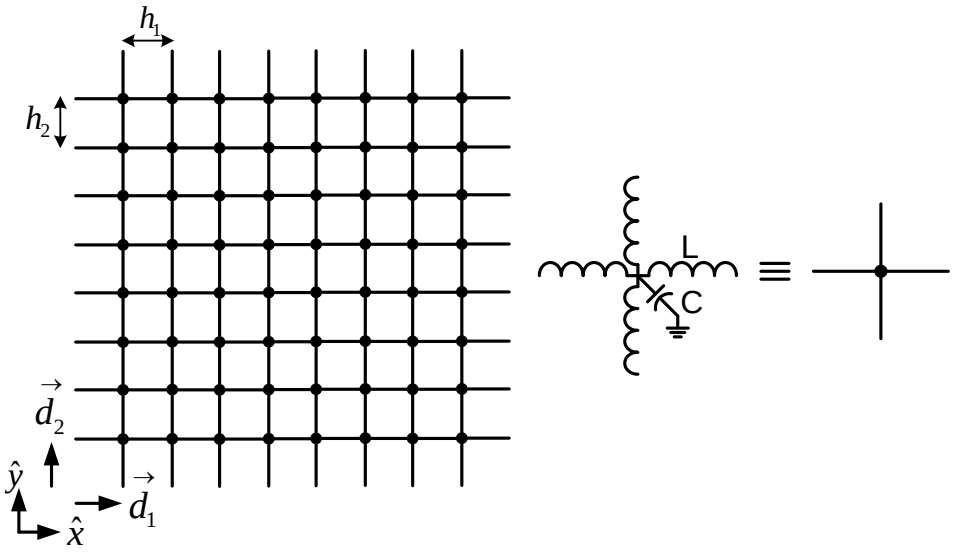

Figure 4.1: Rectangular *LC* lattice.

follows:

$$\vec{d_1} = h_1\hat{x} \tag{4.1a}$$

$$\vec{d_2} = h_2\hat{y} \tag{4.1b}$$

$$\vec{r} = l_1\vec{d_1} + l_2\vec{d_2}. \tag{4.1c}$$

For the above lattice, l_1 and l_2 are integer numbers. For a plane-wave, the voltage at each node is of the form

$$V = A\exp[i(2\pi(\vec{a}.\vec{r}) - \omega t)], \tag{4.2}$$

in which $\vec{a}$ is the wave vector and ω is the angular frequency of the signal. The wave vector directly relates to wave-length λ, and in 2-D it can be defined as

$$\vec{a} = a_1\hat{x} + a_2\hat{y} \tag{4.3a}$$

$$a_1^2 + a_2^2 = 1/\lambda^2. \tag{4.3b}$$

After substituting (4.1) and (4.3) in (4.2), we arrive at the equation:

$$V = A\exp[i(k_1 l_1 + k_2 l_2 - \omega t)], \tag{4.4}$$

where k_1 and k_2 are the phase shifts per section in the $\hat{x}$ and $\hat{y}$ directions respectively. The values of k_1 and k_2 can be by

$$k_1 = 2\pi(\vec{a}.\vec{d_1}) = 2\pi a_1 h_1 \tag{4.5a}$$

$$k_2 = 2\pi(\vec{a}.\vec{d_2}) = 2\pi a_2 h_2. \tag{4.5b}$$

Using the above information, we can find the reciprocal lattice for a rectangular lattice. The reciprocal lattice is an imaginary lattice in the wave-vector space [23]. All of the points in the first Brillouin zone in the reciprocal lattice represent unique $\vec{a}$ vectors. For any point in the second Brillouin zone there is a corresponding point in the first Brillouin zone that represents the same plane-wave. In order to analyze the lattice, it is beneficial to find the reciprocal lattice introduced in [24]. It can be easily shown that the coordinate vectors for the reciprocal lattice are

$$\vec{b_1} = 1/h_1\hat{x} \tag{4.6a}$$

$$\vec{b_2} = 1/h_2\hat{y}. \tag{4.6b}$$

Figure 4.2 shows the reciprocal lattice, along with the first two Brillouin zones for the rectangular lattice. It is apparent from Figure 4.2 that in the first Brillouin zone a_1 and a_2 have the maximum values of $1/2h_1$ and $1/2h_2$, respectively. We can find the maximum values for k_1 and k_2 by:

$$Max\{k_1\} = 2\pi Max\{a_1\}h_1 = \pi \tag{4.7a}$$

$$Max\{k_2\} = 2\pi Max\{a_2\}h_2 = \pi. \tag{4.7b}$$

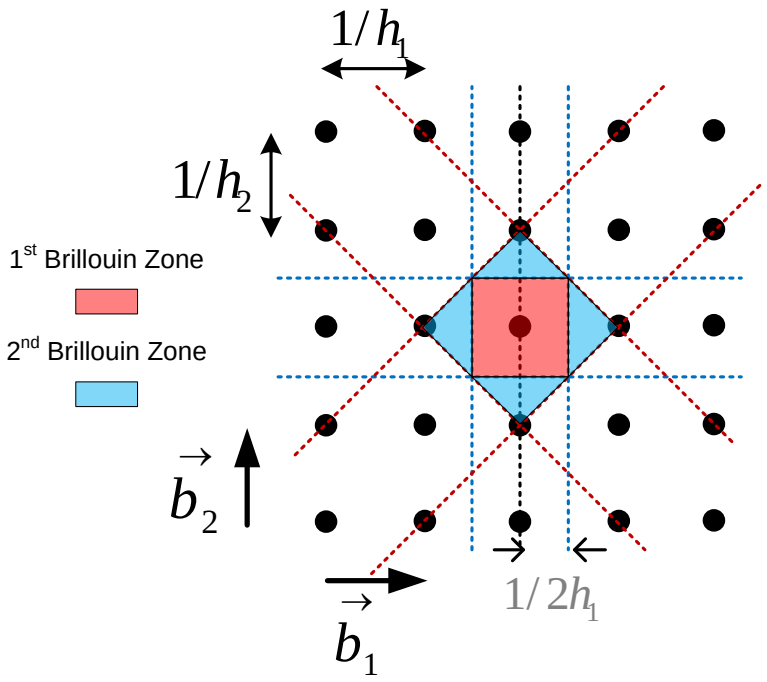

Figure 4.2: Brillouin zones in reciprocal lattice for the rectangular lattice.

To find the direction of the energy in the lattice, the dispersion relation of the lattice needs to be calculated. To do so, we need to first find the differential equation for the lattice cell. Figure 4.3 shows the unit cell for the rectangular lattice. By applying KVL and KCL to the unit cell, we have:

$$LC\frac{d^2V(l_1,l_2)}{dt^2} = V(l_1+1,l_2) + V(l_1-1,l_2) + V(l_1,l_2+1) + V(l_1,l_2-1) - 4V(l_1,l_2). \tag{4.8}$$

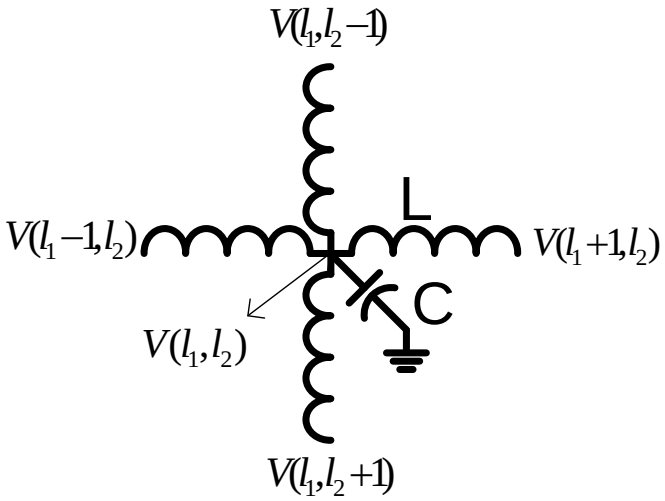

Figure 4.3: Rectangular lattice cell

Now, if a plane-wave voltage of the form (4.4) is assumed for the node voltages in (4.8), it can be shown that the dispersion relation is:

$$\omega = \frac{2}{\sqrt{LC}}\left[\sin^2(k_1/2) + \sin^2(k_2/2)\right]^{1/2}. \tag{4.9}$$

Relation (4.9) shows the nonlinear relationship between the wave vector $\vec{a}$ and the frequency. This fundamentally comes from the discrete nature of the lattice. In electrical lattices usually one of the k_1 or k_2 is defined by the boundary conditions. Figure 4.4 is the plot of k_1 vs. k_2 for different frequencies. This graph is known as the *equi-frequency diagram*. The top right dot in the graph corresponds to the cut-off frequency of the lattice, which is achieved when k_1 and k_2 reach their maximum value:

$$\omega_{cut} = \frac{2\sqrt{2}}{\sqrt{LC}}. \tag{4.10}$$

In a 2-D lattice, the cut-off frequency is a function of the direction of the wave vector. The cut-off frequency in (4.10) is the highest frequency that can propagate in the lattice, and at the cut-off frequency $\angle\vec{a} = \pi/4$ if h_1=h_2. In today's CMOS processes, if we use transmission lines as inductors and metal-to-metal capacitance as capacitors, L and C

values can be as low as 20 pH and 5 fF. This will result in a cut-off frequency of 1.4 THz. Below these values the inductance and capacitance will be dominated by the parasitics.

In a lossless lattice, the energy flow direction is the same as the direction of the group velocity. Using (4.9), group velocity can be shown to be:

$$\vec{V}_g = \nabla_{\frac{k_1}{h_1},\frac{k_2}{h_2}}\omega = h_1\frac{\sin k_1}{\omega LC}\hat{x} + h_2\frac{\sin k_2}{\omega LC}\hat{y}. \tag{4.11}$$

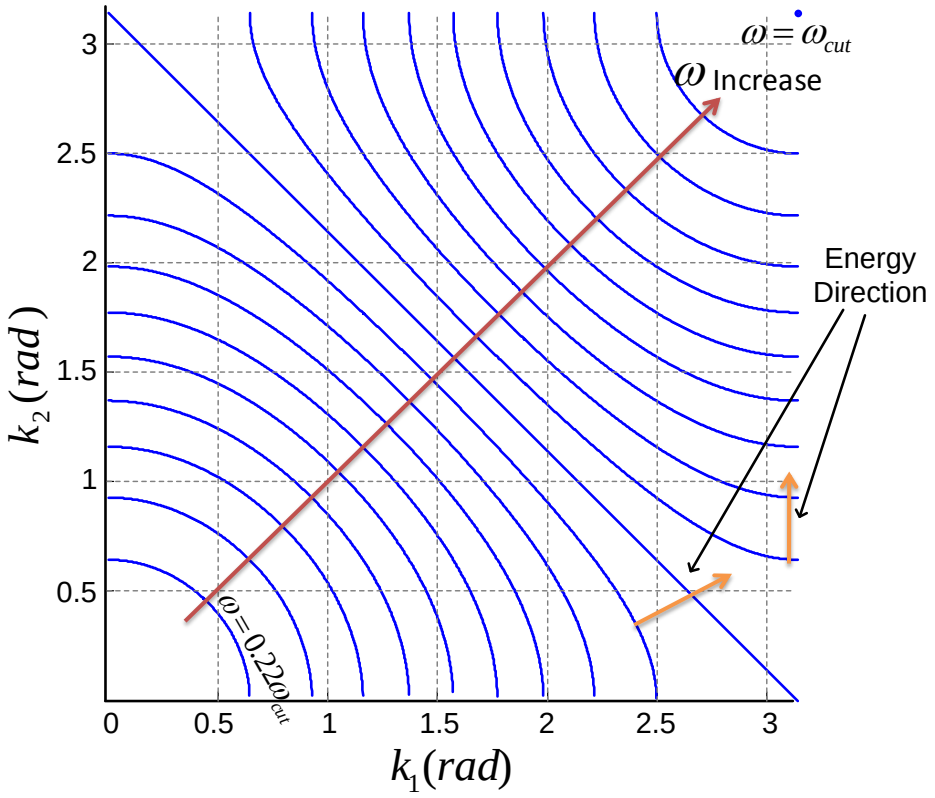

Figure 4.4: Equi-frequency diagram for a rectangular lattice.

From (4.11) the direction of the energy is easily found to be:

$$\text{Energy Direction} = \angle\vec{V}_g = \tan^{-1}\left(\frac{h_2 \sin k_2}{h_1 \sin k_1}\right). \tag{4.12}$$

If $h_1 = h_2$, by definition the group velocity direction is the direction of the perpendicular line to the equi-frequency curves in Figure 4.4. For low frequencies, k_1 and k_2 are small,

and the equi-frequency curves are close to a circle. Therefore, the energy direction is approximately equal to the wave vector $\vec{a}$ direction (e.g. phase velocity direction). The energy direction is specified for two points in Figure 4.4. It is noteworthy to mention that if $h_1 \neq h_2$, even in low frequencies, the energy direction will not be the same as the phase-velocity direction.

It can also be concluded from Figure 4.4 that if k_1 and k_2 are positive–in other words, if $\vec{a}$ has a positive phase between 0 and $\pi/2$–the group velocity $\vec{V_g}$ also would have a phase between 0 and $\pi/2$. This is the reason that the rectangular lattice has a positive effective index over all of the frequencies. Any positive incident angle results in a positive transmission angle in the lattice.

4.2.2 Triangular Lattice

Figure 4.5 shows a right isosceles triangular lattice that is a 45^o rotation of a square lattice. A square lattice is a rectangular lattice in which $h_1 = h_2$. In Figure 4.5, $\vec{d_1}$ and $\vec{d_2}$ are the basis vectors and h_1 and h_2 are the node distances in the $\hat{x}$ and $\hat{y}$ directions, respectively. Because of the symmetry in this lattice, $h_1 = h_2$. For this triangular lattice, we can use exactly the same analysis as in the previous section. The only difference is that in (4.1c) l_1 and l_2 are not integers anymore. To be able to point to all of the nodes with the specified basis vectors, we need to define l_1 and l_2 as follows:

$$\vec{r} = l_1\vec{d_1} + l_2\vec{d_2} \tag{4.13a}$$

$$l_1 = n/2,\ l_2 = m/2,\ n, m = \text{Both Odd or Even.} \tag{4.13b}$$

Having the lattice set up, we can construct the reciprocal lattice for the triangular lattice. Figure 4.6 shows this reciprocal lattice and the Brillouin zones in the lattice. In

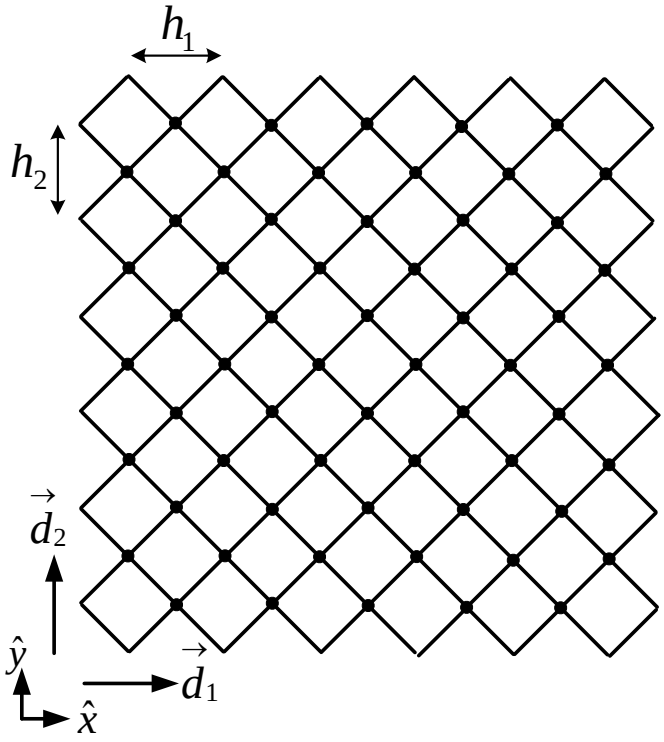

Figure 4.5: Triangular *LC* lattice.

the first Brillouin zone, the maximum values for a_1 and a_2 are $1/h_1$ and $1/h_2$, respectively. Using equation (4.5), we can find the maximum values for k_1 and k_2 in the first Brillouin zone:

$$Max\{k_1\} = 2\pi Max\{a_1\}h_1 = 2\pi \tag{4.14a}$$

$$Max\{k_2\} = 2\pi Max\{a_2\}h_2 = 2\pi. \tag{4.14b}$$

Using the triangular lattice cell in Figure 4.7 and equation (4.4) for a plane-wave, the dispersion relation for a triangular *LC* lattice can be derived as:

$$\omega = \frac{2}{\sqrt{LC}}\left[\sin^2\left(\frac{k_1 + k_2}{4}\right) + \sin^2\left(\frac{k_1 - k_2}{4}\right)\right]^{1/2}. \tag{4.15}$$

The cut-off frequency is the same as (4.10), but when we rotated the lattice by 45^o, $\angle\vec{d} = 0$ or $\pi/2$ instead of $\pi/4$ in a square lattice at the cut-off frequency. Having (4.15) we

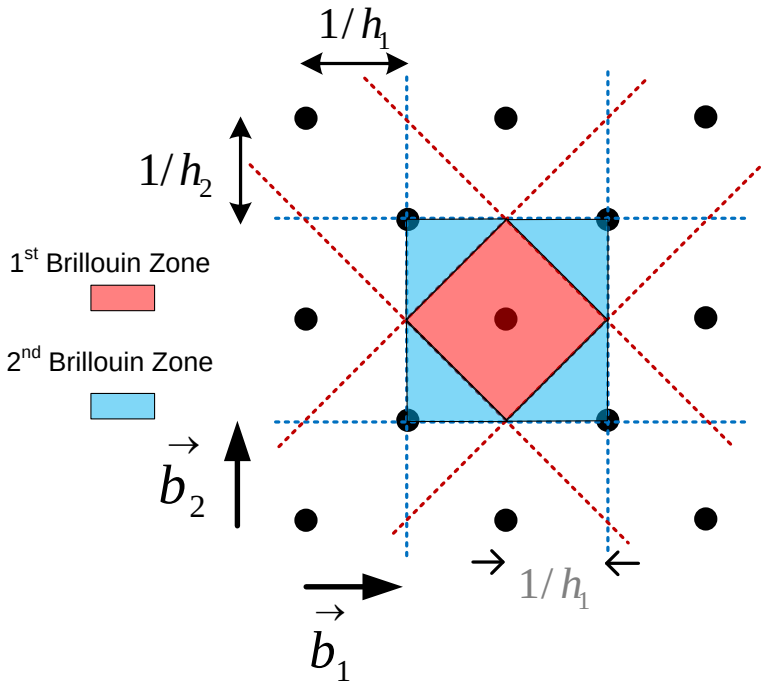

Figure 4.6: Brillion zones in reciprocal lattice for the triangular lattice.

can plot the equi-frequency diagram in Figure 4.8. In this case, there are two solutions for k_1 and k_2 for each frequency. The curves start from $\omega = 0.3\omega_{cut}$ at the upper right and lower left of the graph and end at the points corresponding to $\omega = \omega_{cut}$ at the lower right and upper left of the graph.

Using (4.15) and (4.11), the energy direction in this triangular lattice can be found to be:

$$\angle\vec{V}_g = \tan^{-1}\left(\frac{\sin(\frac{k_1+k_2}{2}) - \sin(\frac{k_1-k_2}{2})}{\sin(\frac{k_1+k_2}{2}) + \sin(\frac{k_1-k_2}{2})}\right). \tag{4.16}$$

In Figure 4.8 the energy direction is specified in two points. For point A, the wave-vector phase, $\angle\vec{a}$, is between 0 and $\pi/2$, as the energy direction. Therefore, at point A the lattice has a positive effective index. This is true as long as k_1 and k_2 are less than π, but as soon as one of them exceeds π, then for positive $\angle\vec{a}$, $\angle\vec{V}_g$ will be negative. This implies a negative effective index for the lattice. Point B is the example of an operating

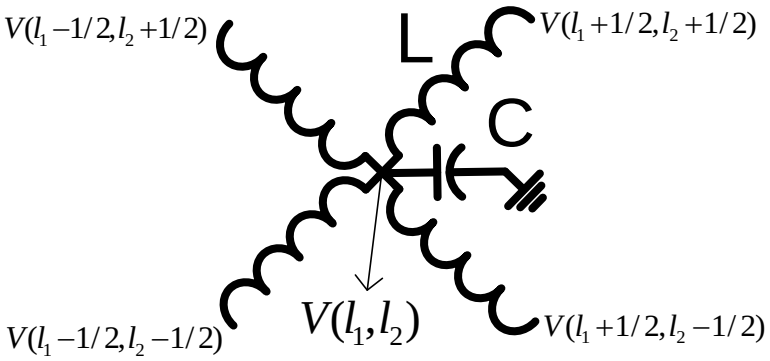

Figure 4.7: Triangular lattice cell.

point in which the lattice has a negative effective index .

4.3 Electrical Prism

4.3.1 Rectangular Lattice + Triangular Lattice

The electrical prism can be made by connecting a rectangular lattice and a triangular lattice together. Figure 4.9 shows the prism in which the rectangular and triangular lattices have a 45^o interface. Different interface angles other than 45^o can also be visualized, but in implementation they are either too complicated or just too big for on-chip realization. In Figure 4.9, the blue lattice is a rectangular lattice and the red lattice is a triangular lattice that is rotated by 45^o. L_1 and C_1 are the inductor and the capacitor for the rectangular lattice, and L_2 and C_2 are the inductor and the capacitor for the triangular lattice.

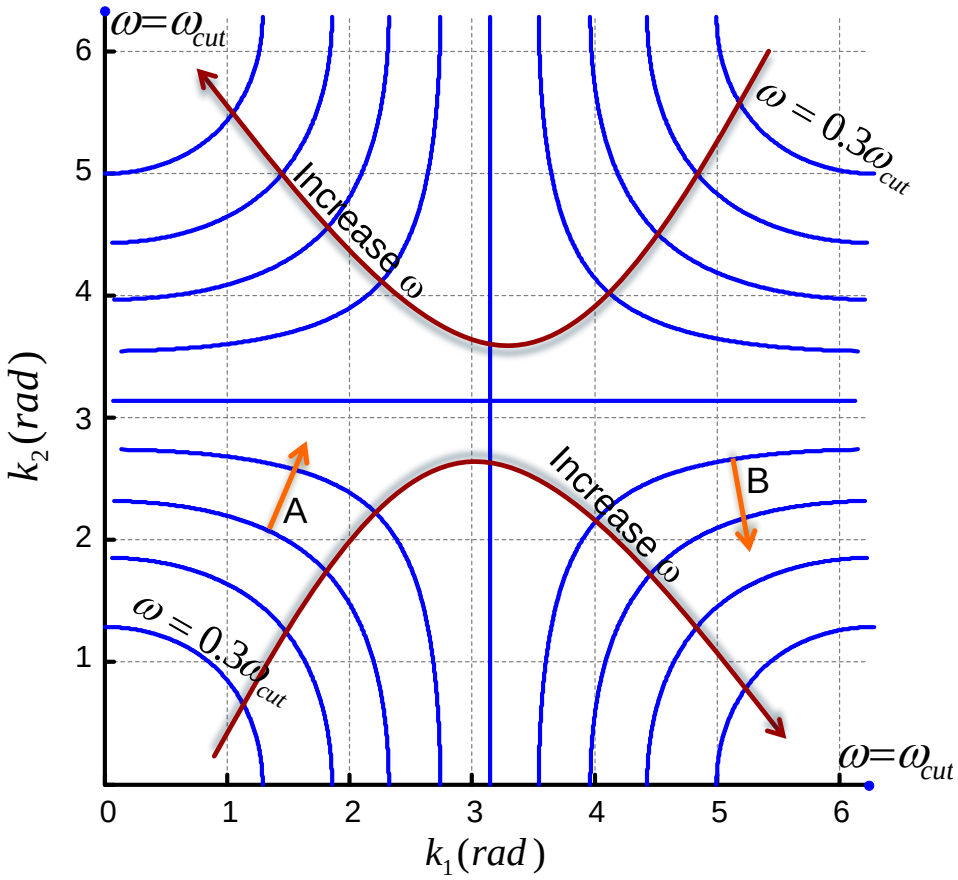

Figure 4.8: Equi-frequency diagram for a triangular lattice.

The plane-wave is flowing from left to right in the rectangular lattice and has an incident angle, θ_i, of 45^o at the interface. The choice of this incident angle eliminates the use of wide-band phase shifters at the boundary and leads to a simpler realization. In Figure 4.9, k_1 and k_2 are the phase shift per section in the rectangular lattice in the $\hat{x}$ and $\hat{y}$ directions, respectively while k_p is the phase shift per section along the interface and k_n is the phase shift per section perpendicular to the interface in the triangular lattice. In both lattices we assume $h_1 = h_2$.

Since $\theta_i = 45^o$, it is clear from Figure 4.9 that $k_2 = 0$. To find the transmission angle,

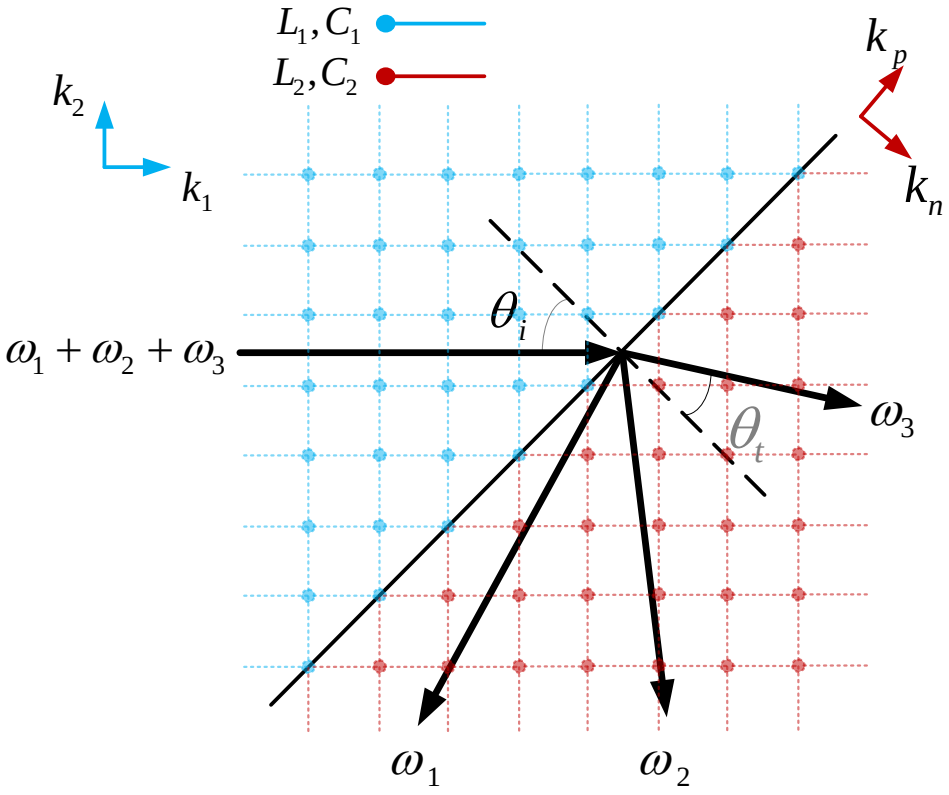

Figure 4.9: Electrical prism using a rectangular and a triangular lattice.

we need to first find k_1. From (4.9), k_1 can be found to be:

$$k_1 = 2\sin^{-1}\left(\omega\sqrt{L_1C_1}/2\right), \tag{4.17}$$

where k_1 is the phase shift per section along the $\hat{x}$ direction in the rectangular lattice. Because the traveling signal is a plane-wave, k_1 is also the phase shift between the consecutive nodes at the lattice interface. In the triangular lattice, k_p is the phase shift per section along the interface, and therefore $k_1 = k_p$. Now, using (4.15) and (4.17), we can find k_n to be:

$$k_n = 2\cos^{-1}\left(\frac{1 - L_2C_2\omega^2/4}{\cos\left(\sin^{-1}\left(\omega\sqrt{L_1C_1}/2\right)\right)}\right). \tag{4.18}$$

Equations (4.17) and (4.18) describe k_p and k_n as a function of lattice components and the signal frequency. In equation (4.16), k_1 and k_2 can be substituted by k_n and k_p, re-

spectively, to find the transmission angle, θ_t. Figure 4.10 is the plot of θ_t vs. signal frequency for different $F = L_2C_2/L_1C_1$. In order to minimize the reflection from the interface, the characteristic impedance of both the lattices should be equal. It is not trivial to calculate the characteristic impedance of a 2-D lattice, especially for frequencies close to the cut-off frequency. The characteristic impedance is a function of the plane-wave propagation direction and is also a function of the signal frequency if it is close to the cut-off frequency. For a rectangular lattice, if the propagation direction is along the $\hat{x}$ or $\hat{y}$ axis, the characteristic impedance is $\sqrt{L/C}$ for low signal frequencies. The characteristic impedance of both lattices is kept constant 50 Ω, and hence $Z_o = \sqrt{L_1/C_1} = \sqrt{L_2/C_2}$ =50 Ω. In Figure 4.10, ω_{cut2} is the cut-off frequency of the triangular lattice. As it was mentioned in the previous section, in today's CMOS processes this cut-off frequency can be as high as 1.4 THz. That is the main reason why this filter can operate at terahertz frequencies.

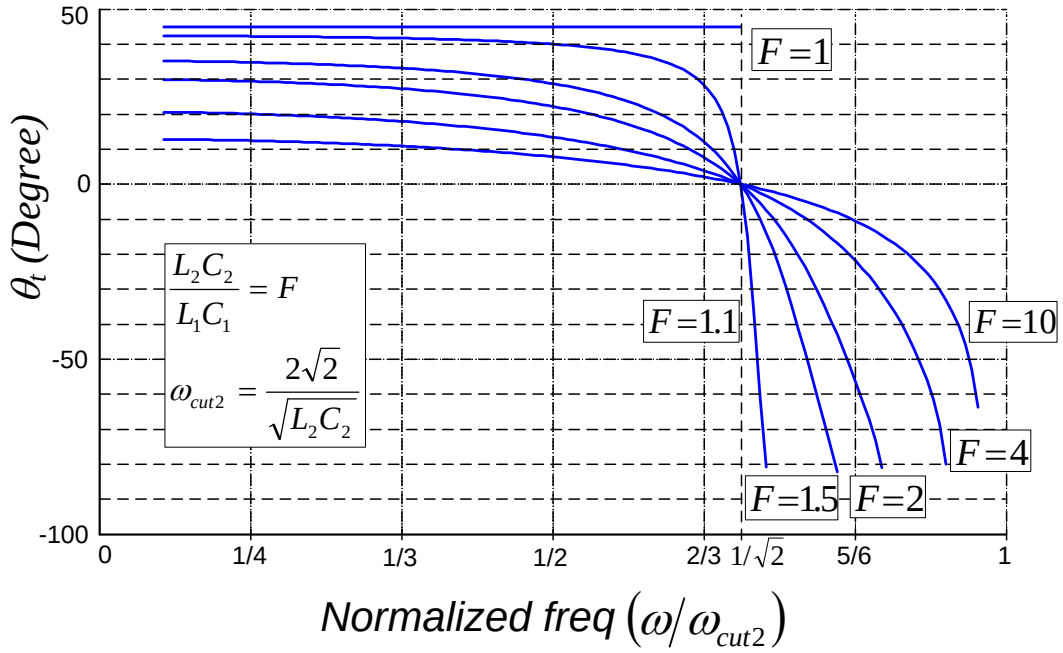

Figure 4.10: Theoretical plot of frequency vs. transmission angle for Figure 4.9.

Figure 4.10 shows that for a specific F factor, as the frequency increases, θ_t and the derivative of the line gets more negative. This suggests that the separation of the frequencies increases at higher frequencies. More frequency separation can also be observed for the lower F factor as the line becomes steeper for those curves. If the output of the filter is fixed to a point on the triangular lattice, more frequency separation translates into a higher quality factor for the filter. The frequency point that all the curves intersect is the cut-off frequency of the triangular lattice when the signal is traveling in the $\hat{x}$ or $\hat{y}$ direction in Figure 4.10. This can be seen in the trivial case of $F = 1$ as the signal stops propagating at the same frequency. The negative effective index is also observed since the incident angle is 45^o and the transmission angle is negative. For low frequencies, the transmission angle reaches a constant number which is the exact angle that we can find from Snell's law:

$$\frac{\sin\theta_i}{\sin\theta_t} = \frac{n_2}{n_1} = \frac{\sqrt{L_2C_2}}{\sqrt{L_1C_1}} = \sqrt{F}. \tag{4.19}$$

This will validate the fact that at low frequencies refraction is the dominant effect in the energy direction but as frequency grows the wavelength becomes comparable to the lattice's dimension and dispersion plays the dominant role in the energy direction.

To validate this theory, a Matlab code is used to solve for the differential equations in the lossless LC lattice and simulate the exact LC circuit. Ten equi-phase sources are applied to the left side of the rectangular lattice to create a plane-wave and the two lattices combined have 60×80 sections. A large lattice is used to better illustrate the direction of the energy. Figure 4.11 shows the profile of the signal as it propagates through both lattices, with the red color the highest and blue the lowest amplitude. The signal frequency is 230 GHz and the F factor is 2 in this figure. The characteristic impedance of both lattices is 50 Ω and the cut-off frequency of the triangular lattice is assumed to be 300 GHz. Therefore, L_2 and C_2 can be calculated to be 75 pH and 30 fF. The propagation direction in Figure 4.11 is defined to be the direction that the maximum amplitude

is traveling. The simulated θ_t is -19^o and the theoretical θ_t from Figure 4.10 is -20^o. The direction of the energy was also simulated for some other frequencies, and they are either exactly the same or just 1^o away from the theoretical value. The 1^o difference can be explained by the transmission angle measurement error in the simulation. Figure

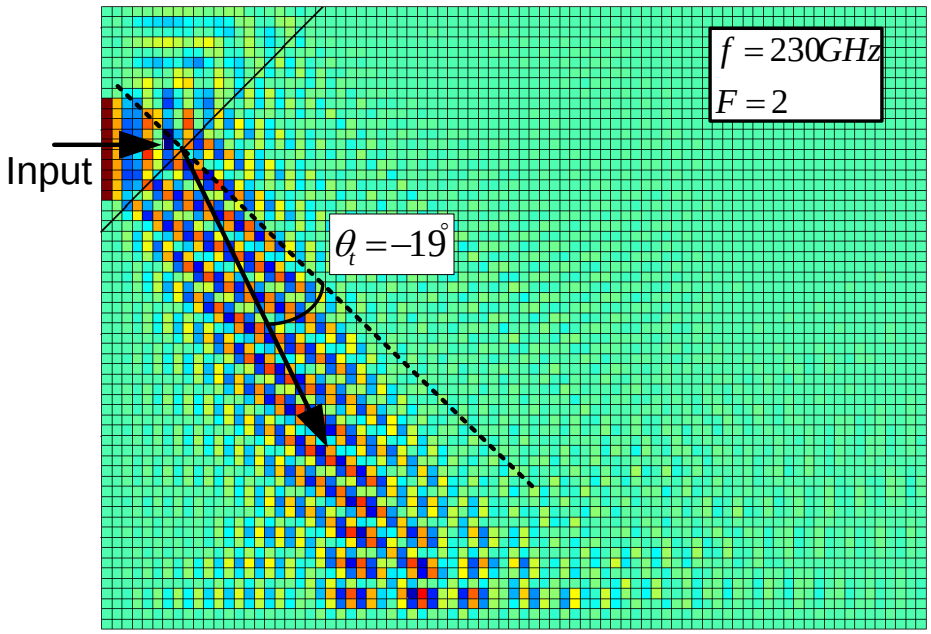

Figure 4.11: Matlab circuit simulation for a lossless lattice.

4.11 also shows the channeling property of the lattice. It can be observed that because the frequency is close to the cut-off frequency the signal is not propagating all over the lattice and channels to a specific direction. Intuitively, because the cut-off frequency is a function of energy direction, the signal dies out faster at directions other than the propagation direction in high frequencies. This has a significant effect on the quality factor of the filter. If the frequency was much lower than the cut-off frequency, as soon as the wave hits the interface all of the nodes would act as point sources and a considerable amount of energy would spread out to most of the output nodes. The width of the signal ray can be defined to be the extent that the amplitude drops 3 dB with respect to the

maximum amplitude. In Figure 4.11 because the lattice is lossless and the frequency is close to the cut-off, the width of the signal ray remains almost constant from the interface to the output. In Section 4.4.2 we will investigate the effect of loss on the width of the signal ray.

To find out the quality factor of the filter, the same lattice was constructed in Cadence. The *LC* section quality factor is chosen to be the typical on chip value of 10 at 230 GHz and the *F* factor is 1.2. The outputs of the filter are four fixed points at the boundary of the triangular lattice. Figure 4.12 shows the normalized gain from input to output for different output nodes. The filter quality factor of 130 is achievable, which is much higher than the component quality factor of 10. This is not possible using classi-

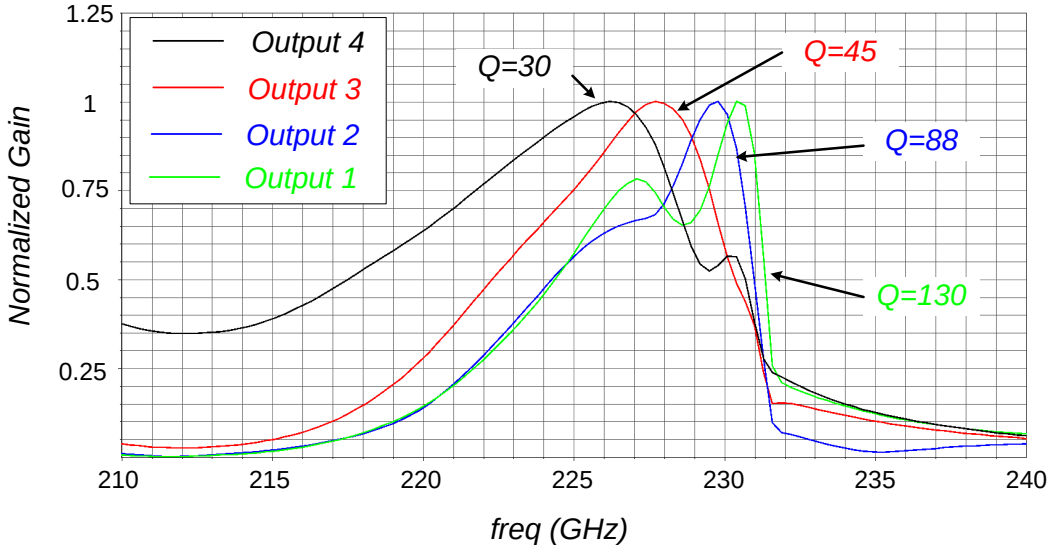

Figure 4.12: Filter Q simulation using Cadence (F=1.2 and *LC* section Q=10)

cal filter design methods. For a given *LC* section quality factor (Q), the quality factor of the filter will be a function of the size of the lattice–the larger the size, the greater the frequency separation, and hence the better the filter quality factor. Of course, the larger the size, the higher the insertion loss would be. Fortunately, the size of the lattice

is scaled down as the frequency of the operation goes up. This is because the inductor value decreases to support the higher frequency and hence reduces the size of the inductor and the overall lattice. This type of lattice is a strong candidate for high-frequency filtering as the Q of the components and the size of the lattice decreases.

4.3.2 Rectangular Lattice + Rectangular Lattice

The electrical prism can also be implemented by connecting two rectangular lattices together. Figure 4.13 shows such a prism with the two rectangular lattices having a 45^o interface. The theoretical analyses are exactly like the one in the previous section. The major difference is that in this kind of filter there will be no negative effective index as two rectangular lattices are being used. So, at low frequencies there will be a constant positive θ_t, and as the frequency increases, θ_t and the slope of the curve will be more positive. Therefore, the filtering and channeling properties still exist, but with a positive transmission angle. There will be two drawbacks for this filter compared with the one in Section 4.3.1. First, the negative θ_t is not present in the filter operation, and hence the span of transmission angle over the frequency range is less than the one in the previous section; this leads to a lower Q for this filter. Second, with respect to a terahertz on-chip implementation, the filter in Section 4.3.1 is simpler to implement because the inductors in both lattices are in the same direction and there is no 45^o angle in the layout.

4.4 The Effect of Component Loss in the Electrical Prism

In order to study the effect of the component loss on the filter quality factor, we should examine its effect on two important features in the electrical prism–the direction of the

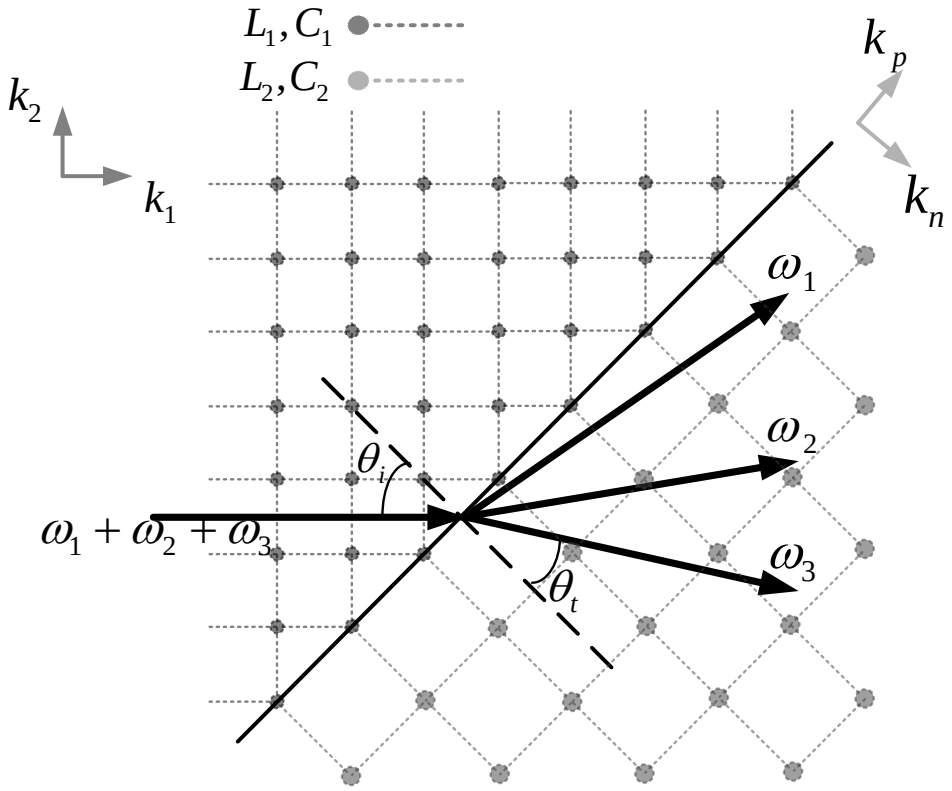

Figure 4.13: Electrical prism using two rectangular lattices.

energy and the channeling effect in the presence of loss.

4.4.1 The Effect of Component Loss on the Direction of Energy

To find the effect of loss on the direction of the energy, we first need to find the dispersion relation of the lattice. Figure 4.14 shows the lossy triangular lattice cell. L and C are the inductor and capacitor values for each section, and R_L and R_C are the resistors in parallel with the inductor and capacitor, respectively. By changing R_L and R_C, we can control the quality factor of the inductor and capacitor independently. Using the same analysis as in the previous section, we can find the dispersion relation for the lossy triangular

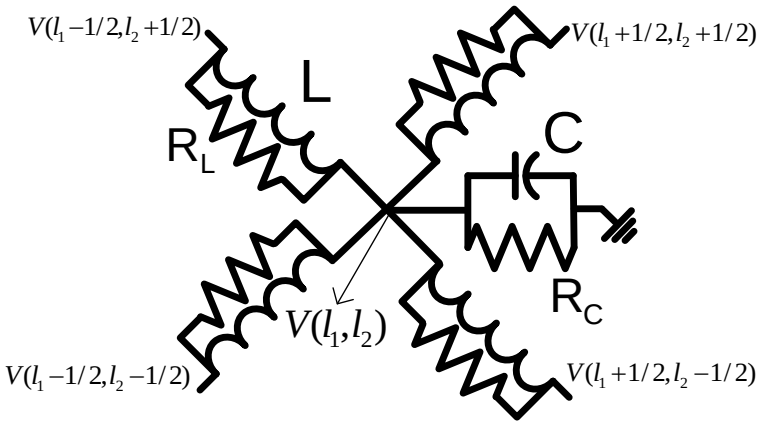

Figure 4.14: Lossy triangular lattice cell.

lattice. The only difference is that the voltage at each node is of the form:

$$V = A\exp[-(\alpha_1 l_1 + \alpha_2 l_2)]\exp[i(k_1 l_1 + k_2 l_2 - \omega t)]. \tag{4.20}$$

where α_1 and α_2 are the attenuation constants in the $\hat{x}$ and $\hat{y}$ directions, respectively. because in the triangular lattice we are using the same inductor everywhere in the lattice, $\alpha = \alpha_1 = \alpha_2$. Using (4.20), we can find the dispersion relation for a lossy triangular lattice:

$$\omega^2 = \frac{4 - (e^{-\alpha} + e^{\alpha})(cos(\frac{k_1+k_2}{2}) + cos(\frac{k_1-k_2}{2}))}{CL + \frac{L^2}{R_L R_C} - \frac{4L^2}{R_L^2} - \frac{L^2(e^{-\alpha} + e^{\alpha})(cos(\frac{k_1+k_2}{2}) + cos(\frac{k_1-k_2}{2}))}{R_L^2}} \tag{4.21}$$

It can be easily verified in the lossless case where R_L and R_C go to infinity, α vanishes and the relation in (4.21) will be the same as the one in (4.15). Having (4.21), we can plot the equi-frequency diagram and compare it with that of a lossless lattice. Figure 4.15 shows the equi-frequency diagram for a lossy lattice in red and the one for a lossless lattice in blue. To plot the curves for a lossy lattice in Figure 4.15, the same 300 GHz cut-off frequency is assumed. L and C are also 75 pH and 30 fF considering the characteristic impedance of 50 Ω. The quality factors of the inductors, Q_L, and the capacitors, Q_C, are chosen to be the typical on chip values of 10 and 100, respectively. This means that

R_L and R_C are changing for each frequency to maintain these chosen values for Q_L and Q_C. Since Q_L is much smaller than Q_C, the LC section quality factor is approximately the same as Q_L=10. Although we have chosen the cut-off frequency in (4.10) to be 300

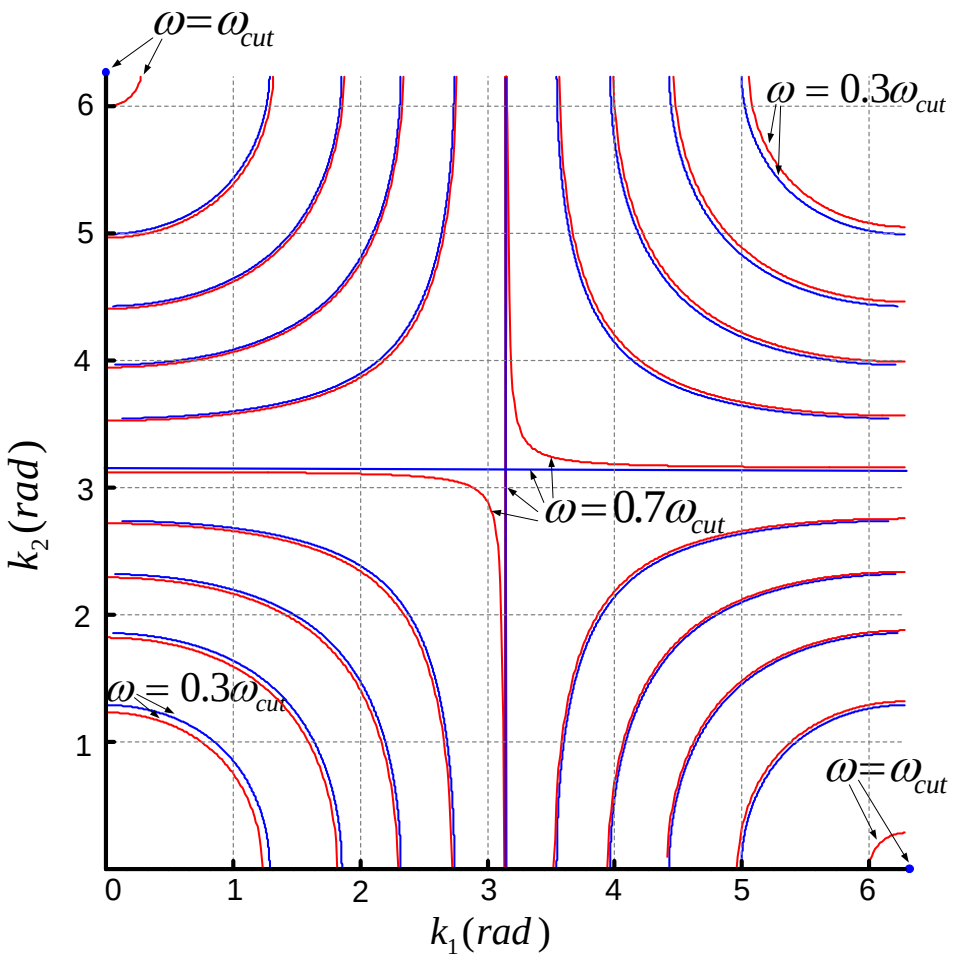

Figure 4.15: Equi-frequency diagram of lossy (red) v.s. lossless (blue) triangular lattice.

GHz, the actual cut-off frequency of the lossy lattice is more than the lossless one. This can be viewed in Figure 4.15 because the red curve for $\omega = \omega_{cut}$ is not a single point anymore. The cut-off frequency in (4.10) is calculated assuming a lossless lattice. The new cut-off frequency for the lossy lattice can be calculated by substituting $k_1 = 2\pi$ and $k_2 = 0$ in (4.21).

As was discussed before, the direction of the energy is the direction of the line perpendicular to the curves in the equi-frequency diagram. For most of the curves in Figure 4.15 the red curve and the blue curve are very similar and close to each other. As the loss is added to the lattice, the curves are slightly shifted to where the lower-frequency curves used to be in the lossless lattice. As a result, the direction of the energy will not change significantly for most of the frequencies. However, the points close to the center of Figure 4.15 may see a significant change in the direction of the energy as the loss is added to the lattice. These points are close to the curve representing $\omega = 0.7\omega_{cut}$ =210 GHz. This frequency is the cut-off frequency of the triangular lattice if $\angle\vec{d} = \pi/4$. Now, if we look at Figures 4.10 and 4.12, we can see that all of the frequencies in which the filter has a high quality factor are larger than 210 GHz. So in conclusion, the direction of the energy for the frequencies of interest would not significantly change as the loss is added to the lattice. Simulation results also verify this fact.

4.4.2 The Effect of Component Loss on the Channeling Effect

It is complicated to theoretically analyze the effect of component loss on the channeling effect. In order to get a sense of what happens to the width of the signal ray in the presence of loss, the filter was simulated with two different *LC* section quality factors. The quality factor of the capacitors kept high in order for the Q_L to be dominant. By comparing the signal profile at the boundary, we can see how wide the signal ray becomes as the component loss changes. In this simulation, signal frequency is 230 GHz and the F factor is 1.2. As before, L_2 and C_2 are 75 pH and 30 fF. The result of this simulation in Figure 4.16 is the plot of normalized voltage amplitudes for different outputs at the boundary. The narrower this voltage profile is, the more channeled is the signal ray. It is clearly shown that for the higher component quality factor the signal profile is narrower,

and hence more channeling is acquired. The narrower the signal ray, the higher is the filter quality factor that is achievable.

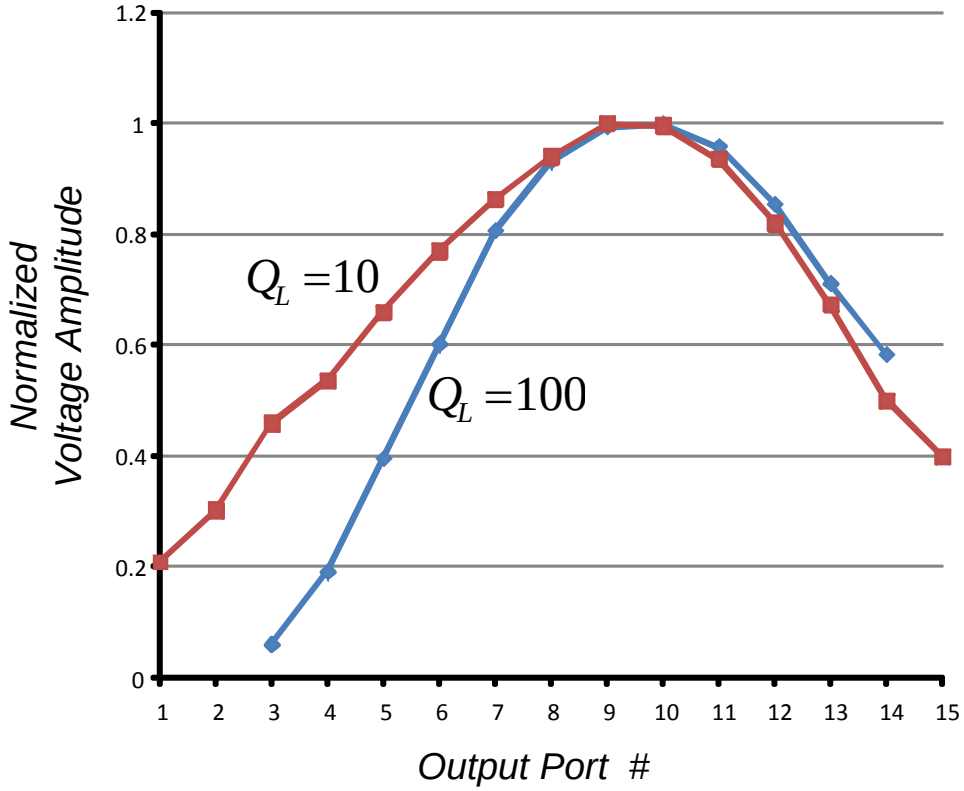

Figure 4.16: Normalized voltage amplitude v.s. different output nodes for inductor quality factors of 10 and 100.

4.4.3 Filter Quality Factor vs. Component Quality Factor

Figure 4.17 shows the filter quality factor vs. the LC section quality factor for different frequency bands. The ratio of *LC* product in two lattices, F, is kept constant at 1.2 for all four frequencies. As before, L_2 and C_2 are 75 pH and 30 fF for the 230 GHz. For the frequencies 460 GHz, 115 GHz and 57 GHz, L_2 and C_2 are multiplied by half, two and four, respectively. To have a fair comparison, the physical size of the lattice is kept

constant for all three frequencies. This means that the number of sections is reduced for lower frequencies to keep the same die size. We used 95×35 sections for 460 GHz, 60×30 sections for 230 GHz, 38×25 sections for 115 GHz and 25×20 sections for 57 GHz. As a result, for a constant *LC* quality factor the filter quality factor drops as the frequency drops. It is apparent from Figure 4.17 that for a constant frequency the filter quality factor decreases as the component quality factor drops. This is expected because the channeling effect decreases as the component loss increases. This simulation shows that it is possible to get a quality factor of 420 at 460 GHz with a *LC* section quality factor of 20. The 460 GHz curve is not plotted for *LC* section quality factor less than 15. The low quality factor along with the many lattice sections at 460 GHz causes the loss to be high and hence the filter to loose the frequency separation at different outputs. This means the filter is not working properly when *LC* section quality factor is less than 15 and the filter quality factor in not meaningful in comparison to other point in the graph. Two important points can be derived from Figure 4.17:

- For a constant die size, higher frequency filters will result in higher quality factors for the filters.
- We will achieve a higher quality factor boost ratio (the ratio of filter Q over component Q), for the component quality factor of less than 20.

4.5 Electrical Prism Implementation

A 0.13 μm CMOS process with seven metal layers was chosen to implement the electrical prism. As was discussed earlier, for the same filter quality factor, the size of the lattice decreases as the frequency increases. Thus, for the proof of concept it is reasonable to choose the highest possible frequency to reduce the size as much as possible. A

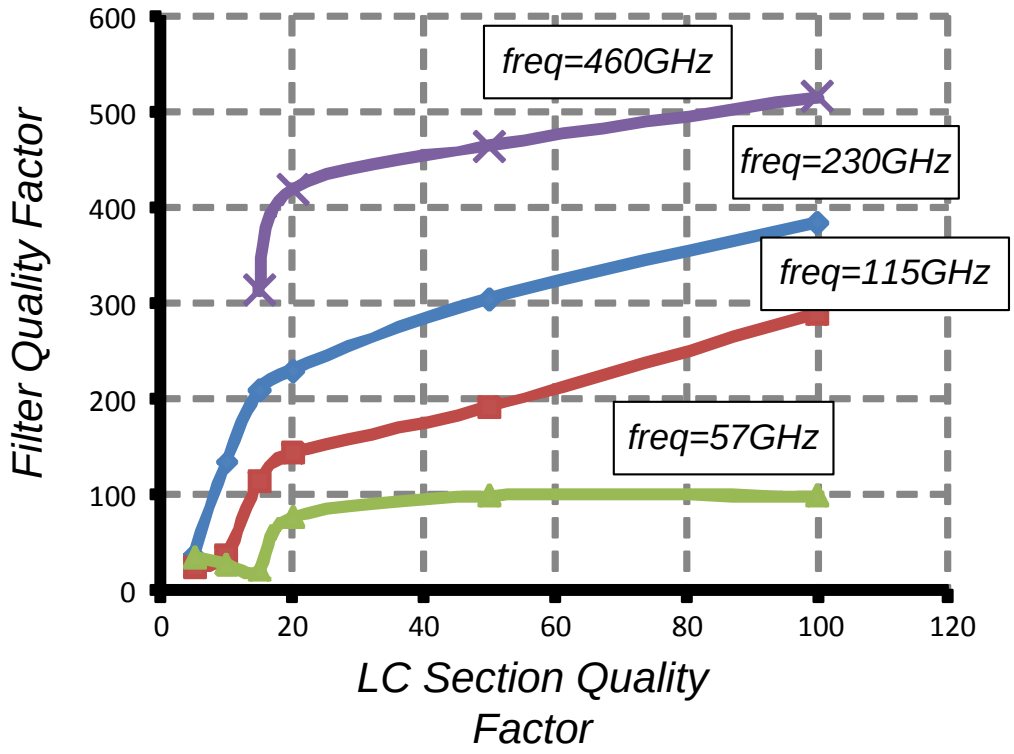

Figure 4.17: Filter quality factor vs. component quality factor.

maximum frequency of 50 GHz was chosen due to the availability of the measurement tools and a relatively easier measurement setup compared with that of higher frequencies. To have high quality factor inductors, 100 μm×100 μm spiral inductors were used for both rectangular and triangular lattices. The available die size of 3.5 mm×2.5 mm along with the inductor size, defines the number of sections to be 18×11 for the electrical prism. The *LC* section quality factor is limited to the inductor quality factor in the 50 GHz range. At this frequency, the typical quality factor value for the spiral inductors in this process is around 20. Now, if we look at Figure 4.17, for the 57 GHz curve we will get a filter quality factor of 70 if we use an inductor with a quality factor of 20. But for our implementation, both the frequency and the lattice size are smaller than the 57 GHz curve in Figure 4.17. Therefore, a filter quality factor of significantly less than 70

is expected, even with $F = 1.2$ which was used in Figure 4.17. Based on Figure 4.10, if a lower F factor is used, higher filter quality factor is achievable. But an F factor less than 1.2 is not safe to use because the filter operation will be very sensitive to process variation. From Figure 4.10, we know for $F = 1.2$, useful filtering is happening roughly between $0.7\omega_{cut}$ and $0.8\omega_{cut}$. Because our maximum measurable frequency is 50 GHz, $0.8\omega_{cut}$ =50 GHz. This will result in a triangular lattice cut-off frequency of around 60 GHz. For a cut-off frequency of 60 GHz and a characteristic impedance of 50 Ω, the inductor size for the triangular lattice will be 375 pH. In this process, the quality factor of a 375 pH inductor is around 10 for 50 GHz applications. In order to reduce the loss of the lattice, the characteristic impedance was reduced to 30 Ω. Now, the inductor size is 230 pH and the quality factor is around 20. In order to probe the signals at the input and output of the lattice, impedance-matching circuits were used to match 30 Ω to 50 Ω. The implemented electrical prism is shown in Figure 4.18. A wide-band, one-to-eight power divider was designed to generate the eight equi-phase sources at the boundary of the rectangular lattice. Simulation shows that eight signal sources are good enough to generate a plane-wave in the rectangular lattice. A 50 GHz signal source is used to apply the input signal to the lattice through the GSG pads. As was mentioned, the inductors and capacitors for the triangular lattice are designed to be L_2 =230 pH and C_2 =250 fF. The inductors were implemented using spiral inductors with a quality factor of 20, and the capacitors were realized using MOS capacitors to get a quality factor of 80 for 50 GHz frequency. The outputs are probed at the bottom boundary of the triangular lattice through GSG pads. Five outputs is the maximum number we could have, given the size of the pads. In Figure 4.18, The higher-frequency signals flow to $Vo1$, and the lower-frequency signals can be probed at $Vo5$. The attenuation constant for the higher-frequency signals flowing into $Vo1$ is higher than the one at $Vo5$. Therefore, to equalize the voltage amplitudes at different outputs the boundary was tilted. As is shown in Fig-

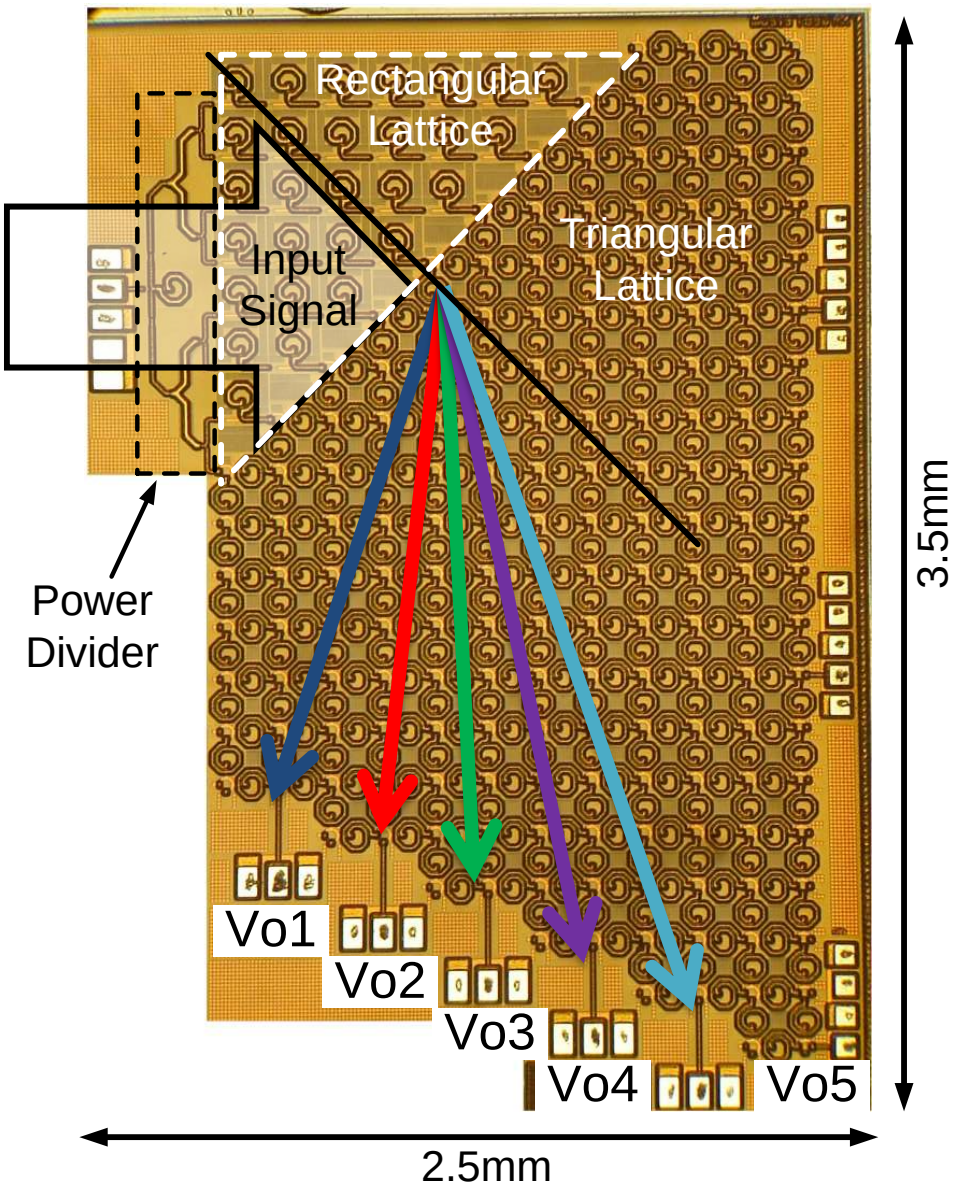

Figure 4.18: Die picture.

ure 4.17, if the number of sections in the lattice and the component quality factor are low, having a low F factor will not improve the filter quality factor significantly. Thus the F factor was optimized to get smooth filtering properties without sacrificing the filter quality factor. The best F is found to be 2.6. As a result, the inductors and capacitors for the rectangular lattice will be L_1 =145 pH and C_1 =150 fF. In the rectangular lattice, the

vertical sections were removed to simplify the implementation but that will not change anything because no signal is flowing into those sections.

Figure 4.19 shows the simulation results for the five output nodes. The graph shows the normalized gain from input to each output vs. signal frequency. To better illustrate the frequency shift of the peaks, the normalized gain was used. All of the peaks for the outputs are within 20% of the highest one in $Vo5$ due to the boundary tilting. The signal peaks at about 34.5 GHz and 38.5 GHz for $Vo5$ and $Vo1$, respectively. Figure 4.19 clearly shows the filtering behavior of the lattice and verifies the negative effective index for the lattice. The filter quality factors vary from 8 to 12 for different outputs. This is expected, based on the above discussion. $Vo1$ has the highest and $Vo5$ has the lowest filter quality factor. The insertion loss from each source at the boundary to each output is about 20 dB.

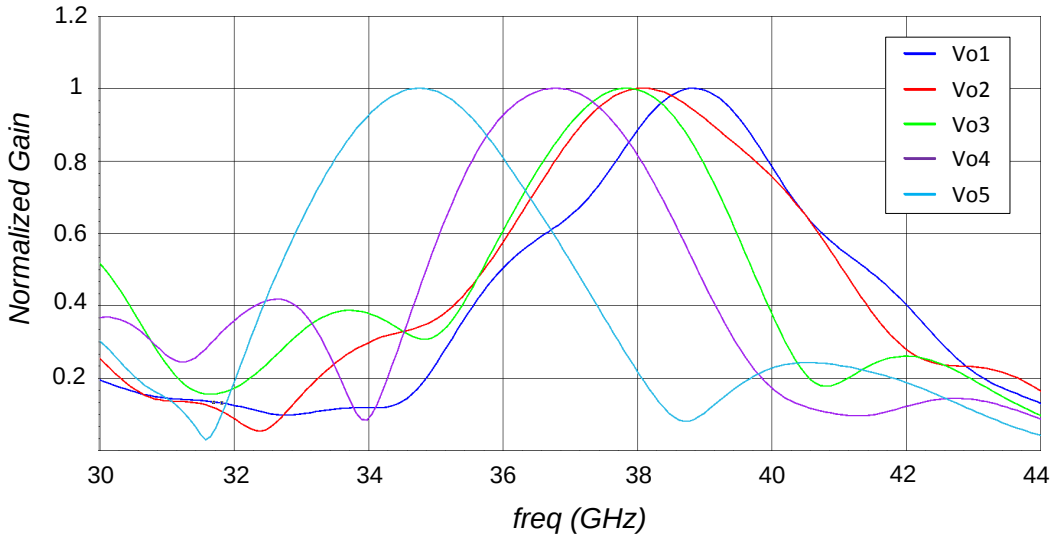

Figure 4.19: Gain simulation results from input to each output.

Figure 4.20 presents the measurement results for the five output nodes. The results are very close to the simulation results. The peaks for different outputs are distributed

over a 4 GHz span, as was done for the simulation in Figure 4.19. Similarly, the peaks for all of the outputs are within 20% of the highest one. The filter quality factors is also very close to simulation and changes from 8 to 12 for different outputs.

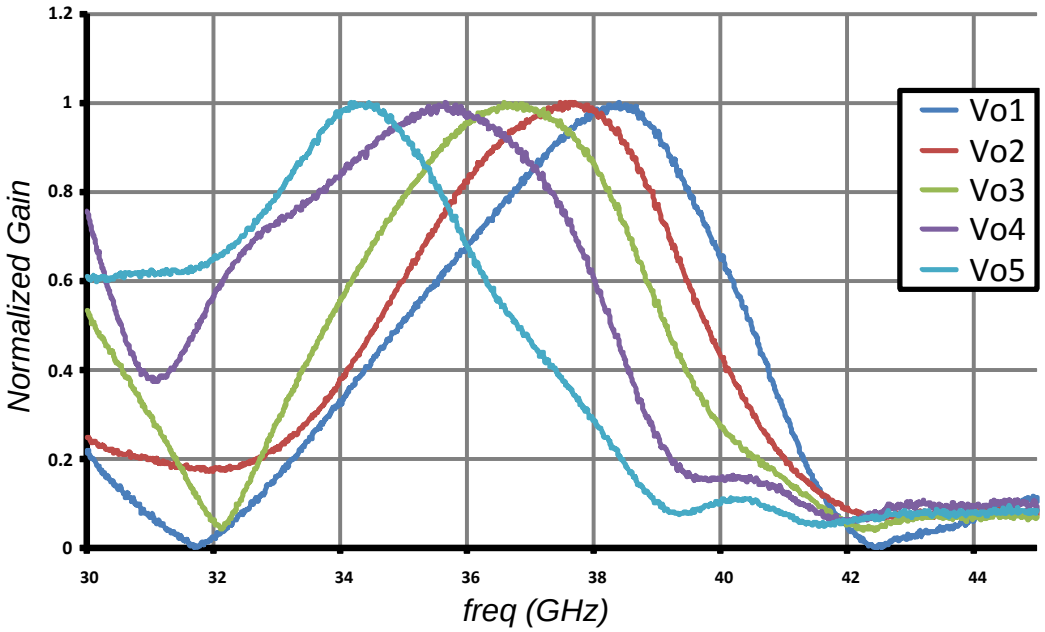

Figure 4.20: Gain measurement results from input to each output.

4.6 Conclusion

Energy direction is a function of frequency in low-pass 2-D lattice at frequencies close to the cut-off. This property can be exploited by implementing a high quality factor filter called an electrical prism. Negative effective index was shown to be achievable using the structure. Channeling of the signal and spatial filtering are the main reasons behind the filter having a higher quality factor than component quality factors. Considering a fixed die size, the filter achieves higher quality factor values for terahertz frequencies. A prototype was designed and measured to prove the feasibility of this approach. This

structure is especially interesting because it is easy to fabricate using a conventional CMOS process.

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